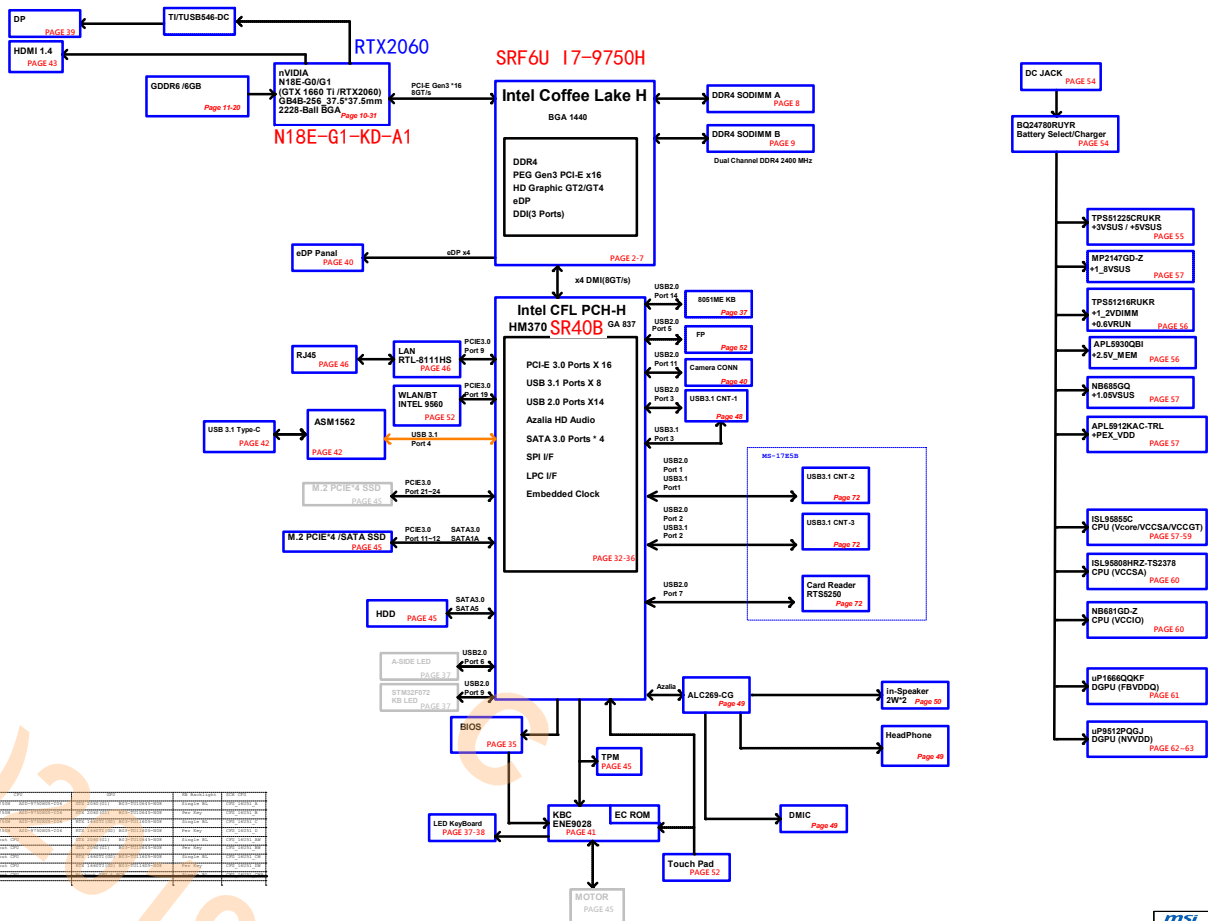
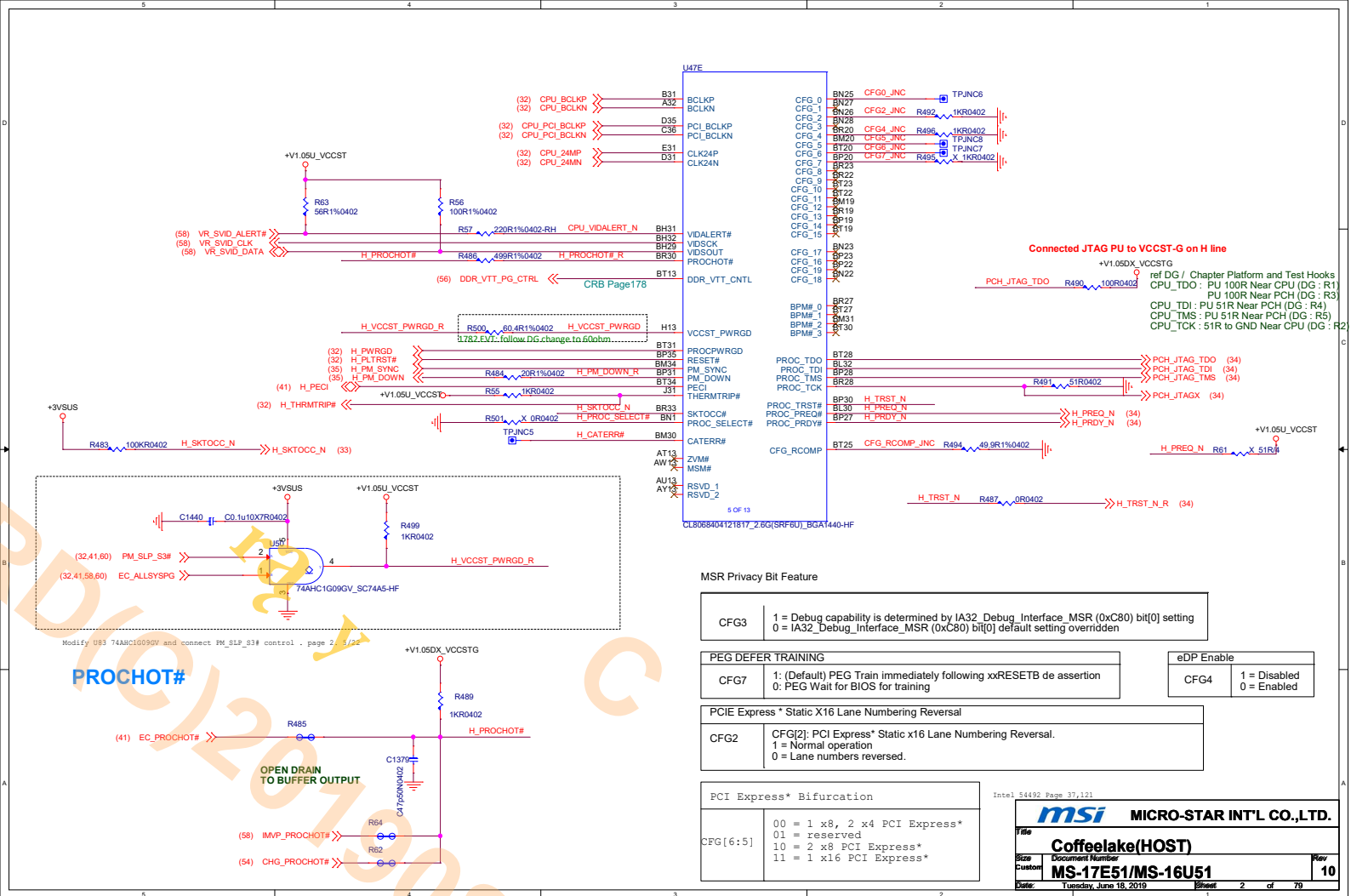


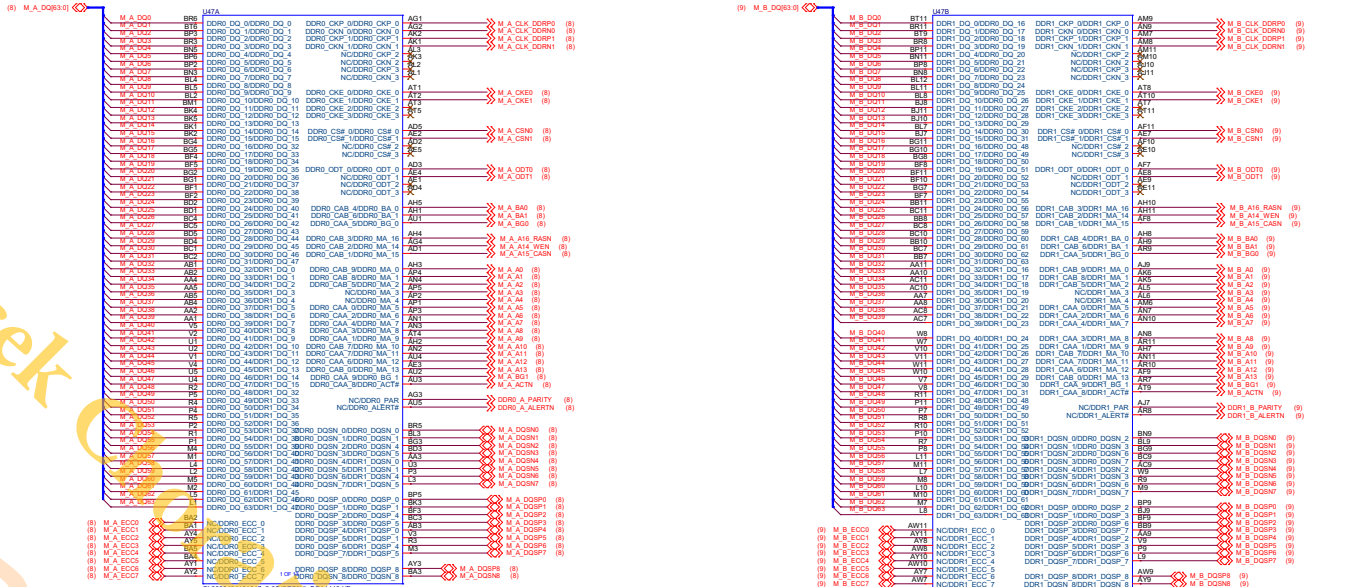
Page 01: Block Diagram
Page 02: CoffeeLake(PCHT)
Page 03: CoffeeLake(DDR4)
Page 04: CoffeeLake(DMI/Display)
Page 05: CoffeeLake(Power1)
Page 06: CoffeeLake(Power2)
Page 07: CoffeeLake(Power3)
Page 08: CoffeeLake(Power4)
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Page 10: DGPU FCH Host
Page 11: DGPU MEM IF A/B
Page 12: DGPU GDDR6 FrameBuffer A0
Page 13: DGPU GDDR6 FrameBuffer A1
Page 14: DGPU GDDR6 FrameBuffer B0
Page 15: DGPU GDDR6 FrameBuffer B1
Page 16: DGPU MEM IF C/D
Page 17: DGPU GDDR6 FrameBuffer C0
Page 18: DGPU GDDR6 FrameBuffer C1
Page 19: DGPU GDDR6 FrameBuffer D0
Page 20: DGPU GDDR6 FrameBuffer D1
Page 21: DGPU PWR AND GND
Page 22: DGPU PWR AND GND
Page 23: DGPU GPU DECOUPLING A
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Page 25: DGPU DAC/Display IF
Page 26: DGPU NVLink & Framelock
Page 27: DGPU GPIO I2C
Page 28: DGPU ROM/HW Straps
Page 29: DGPU MIO & XTAL
Page 30: DGPU Power Control
Page 31: DGPU Power control, Discharge
Page 32: FCH CLK/DIO
Page 33: PCH 2(USB/SATA/PCIe)
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Page 55: System Power
Page 56: +1.2VDDIMM/+0.6VVRUN/+2.5V MEM
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Page 58: CPU Power (ISUS55)
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Page 74: B(CS0.1)
Page 75: B(History)
Page 76: C(Power Switch)
Page 77: C(History)
Page 78: TOP
Page 79: Bottom VIEW

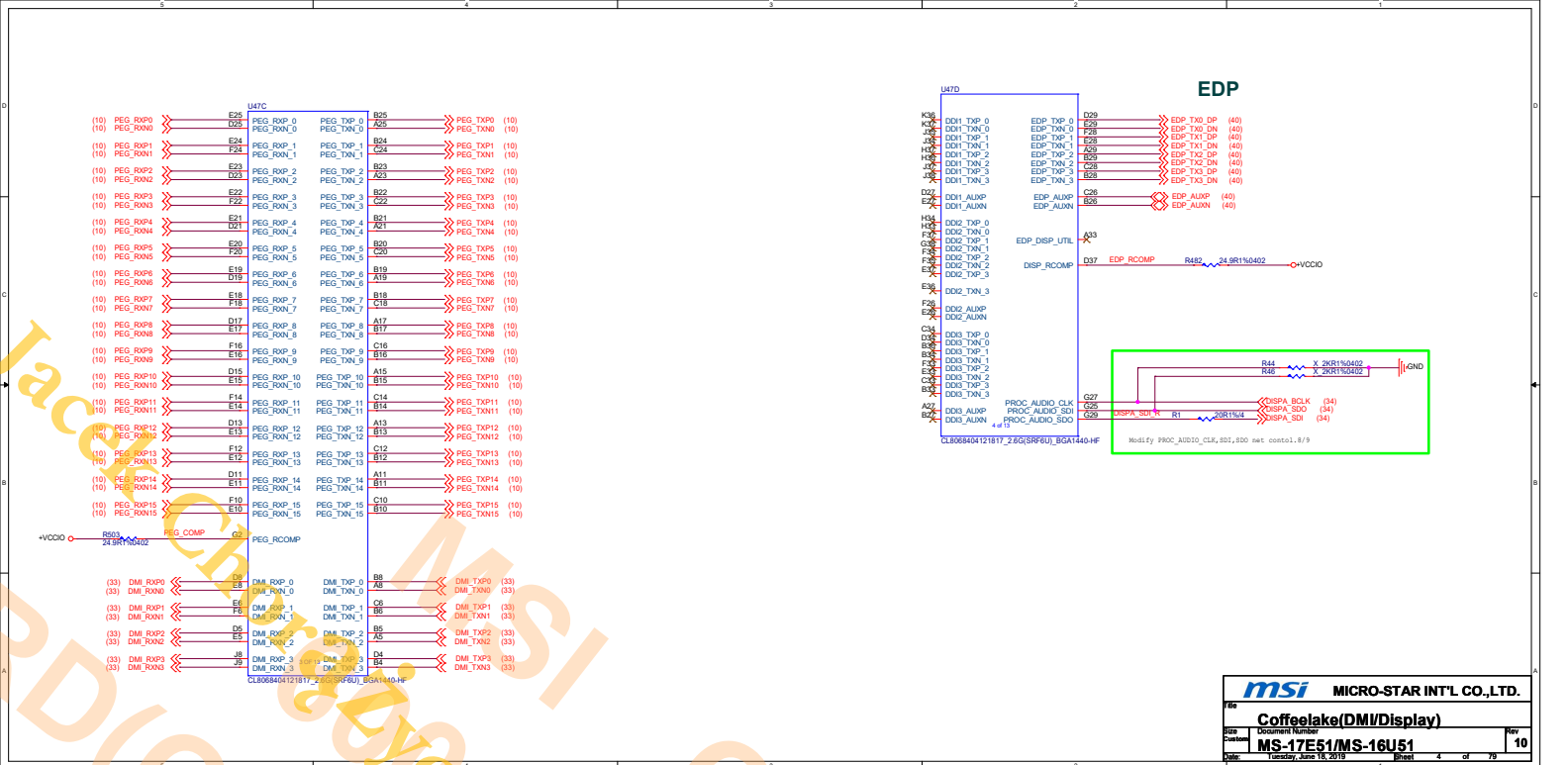


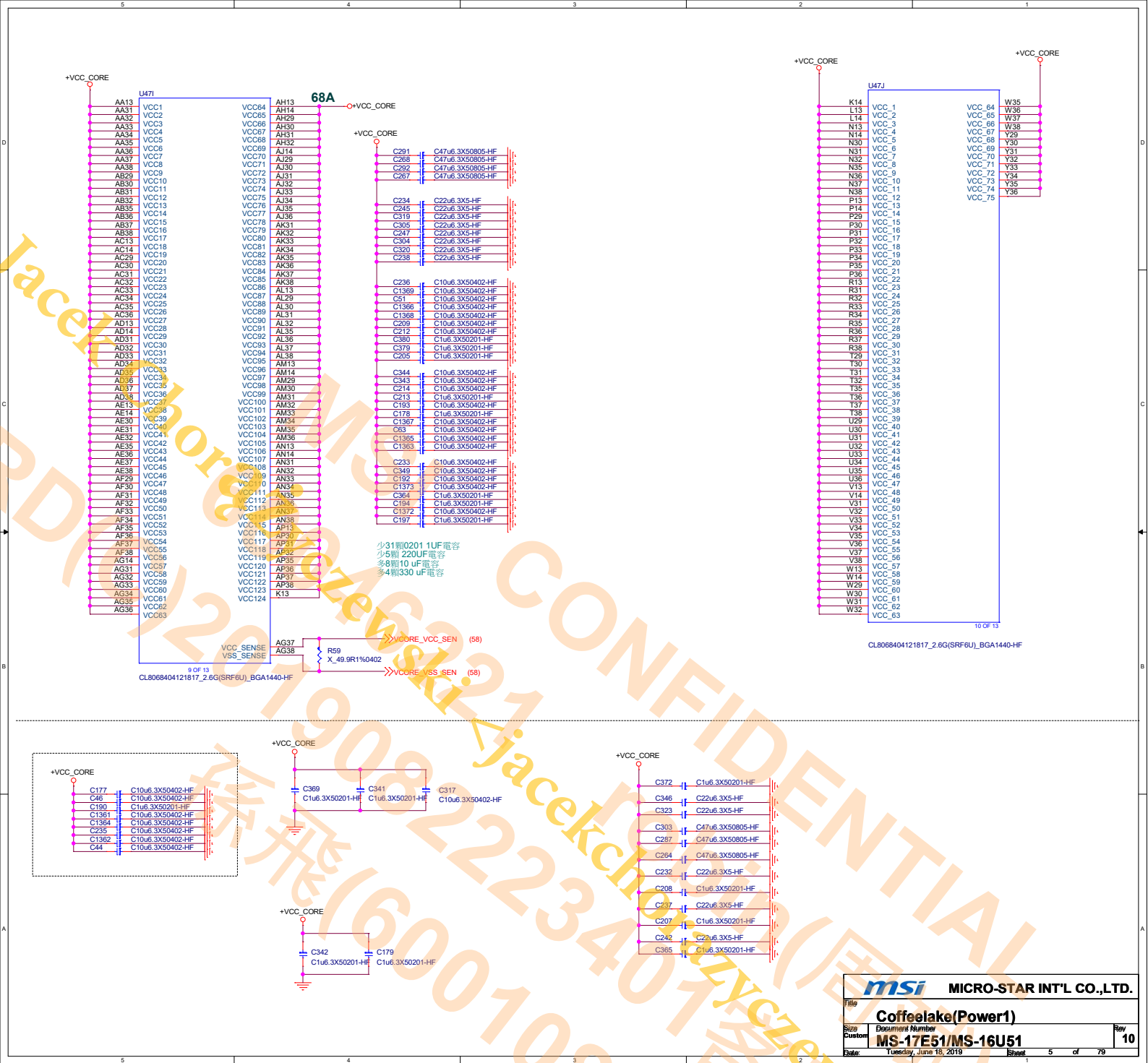


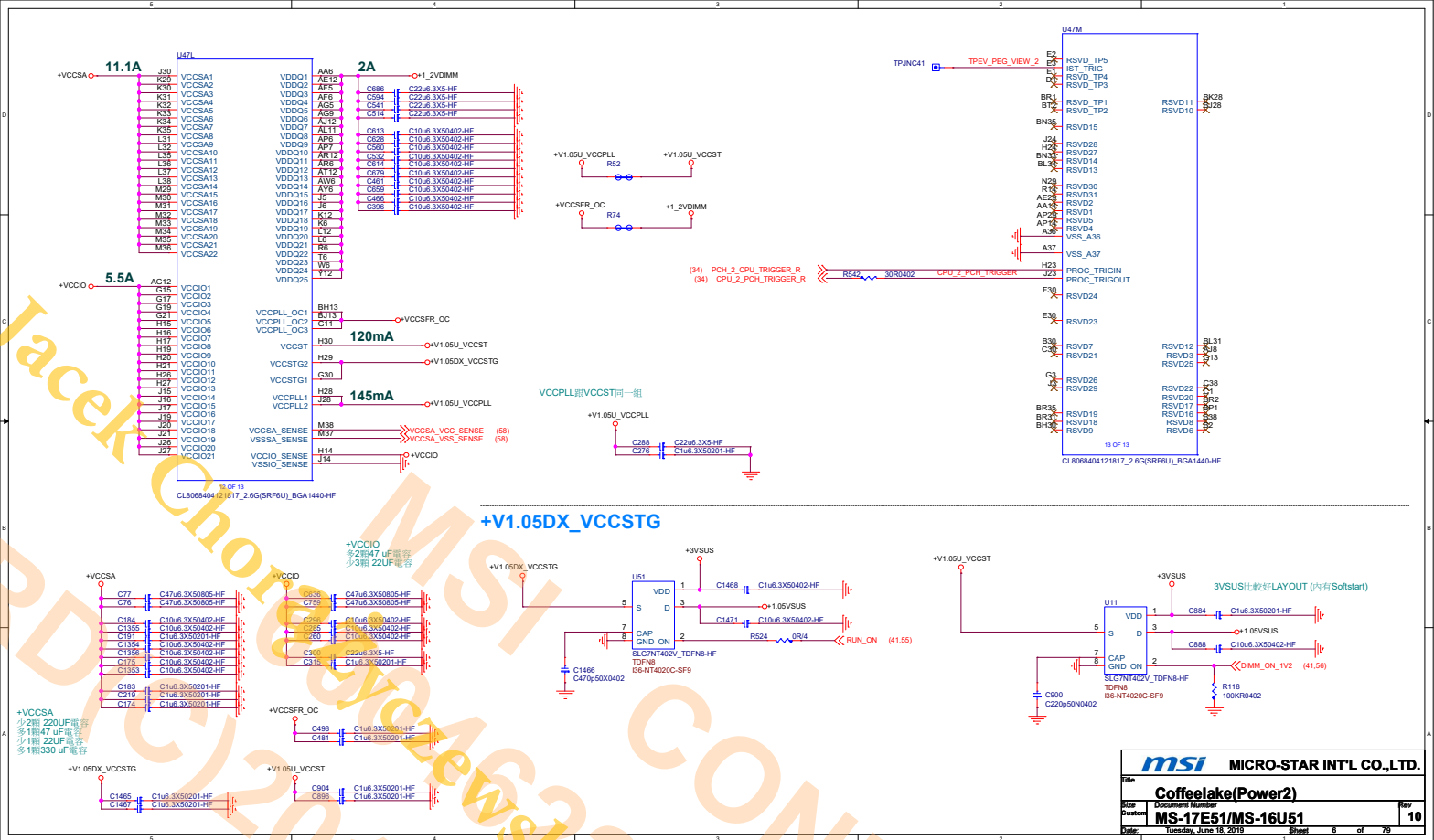
DDR Channel A

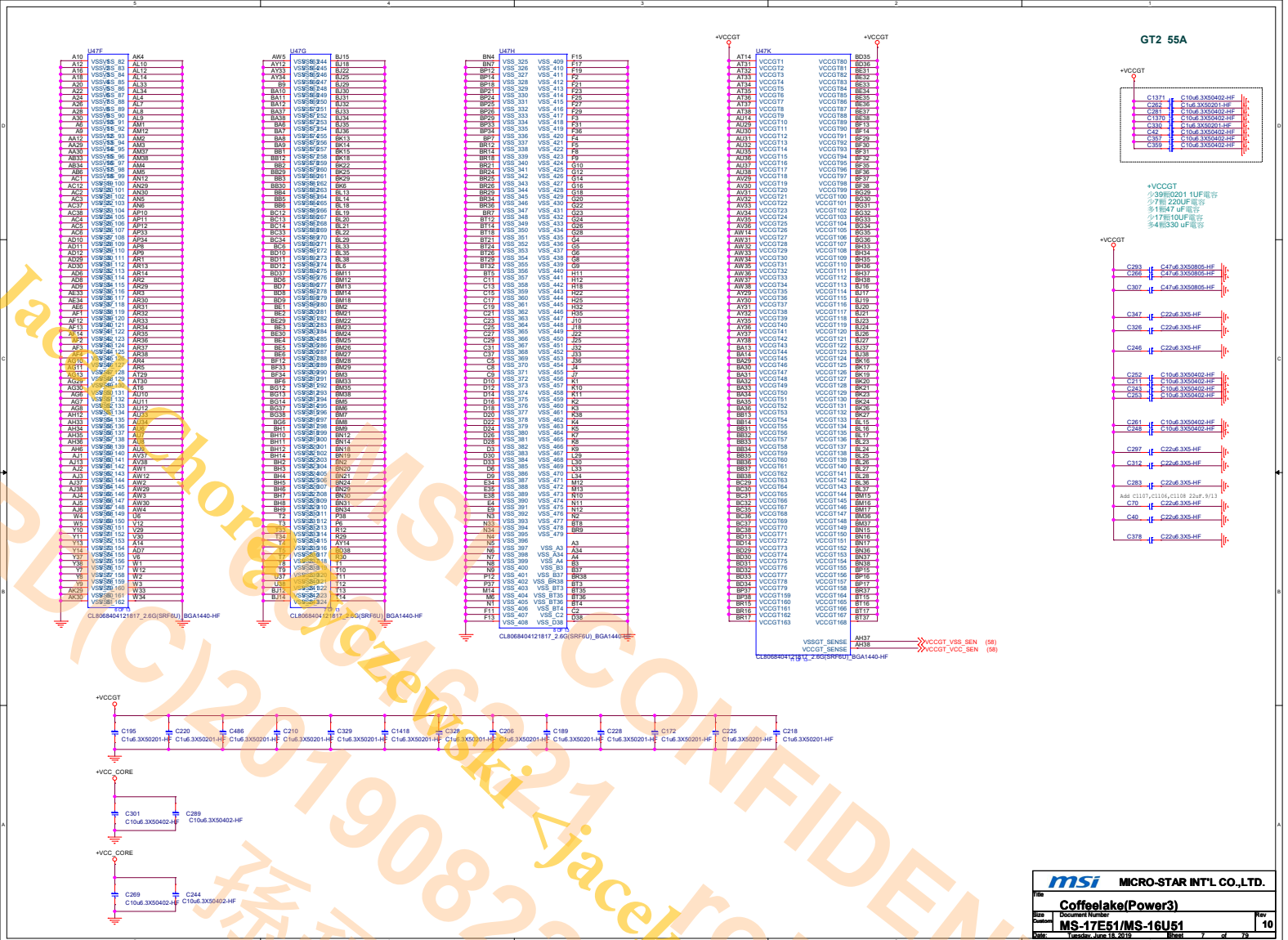
DDR Channel B

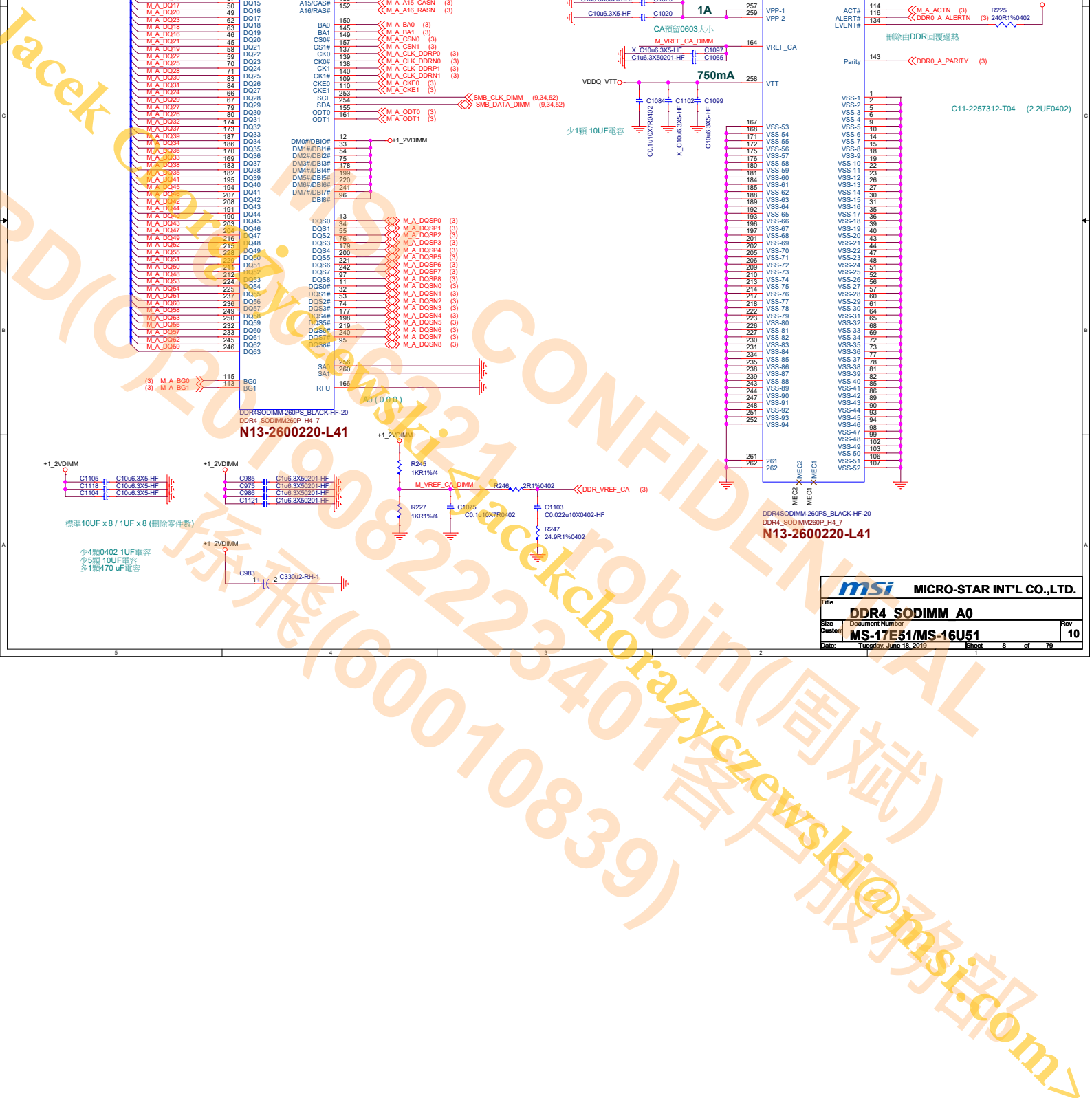




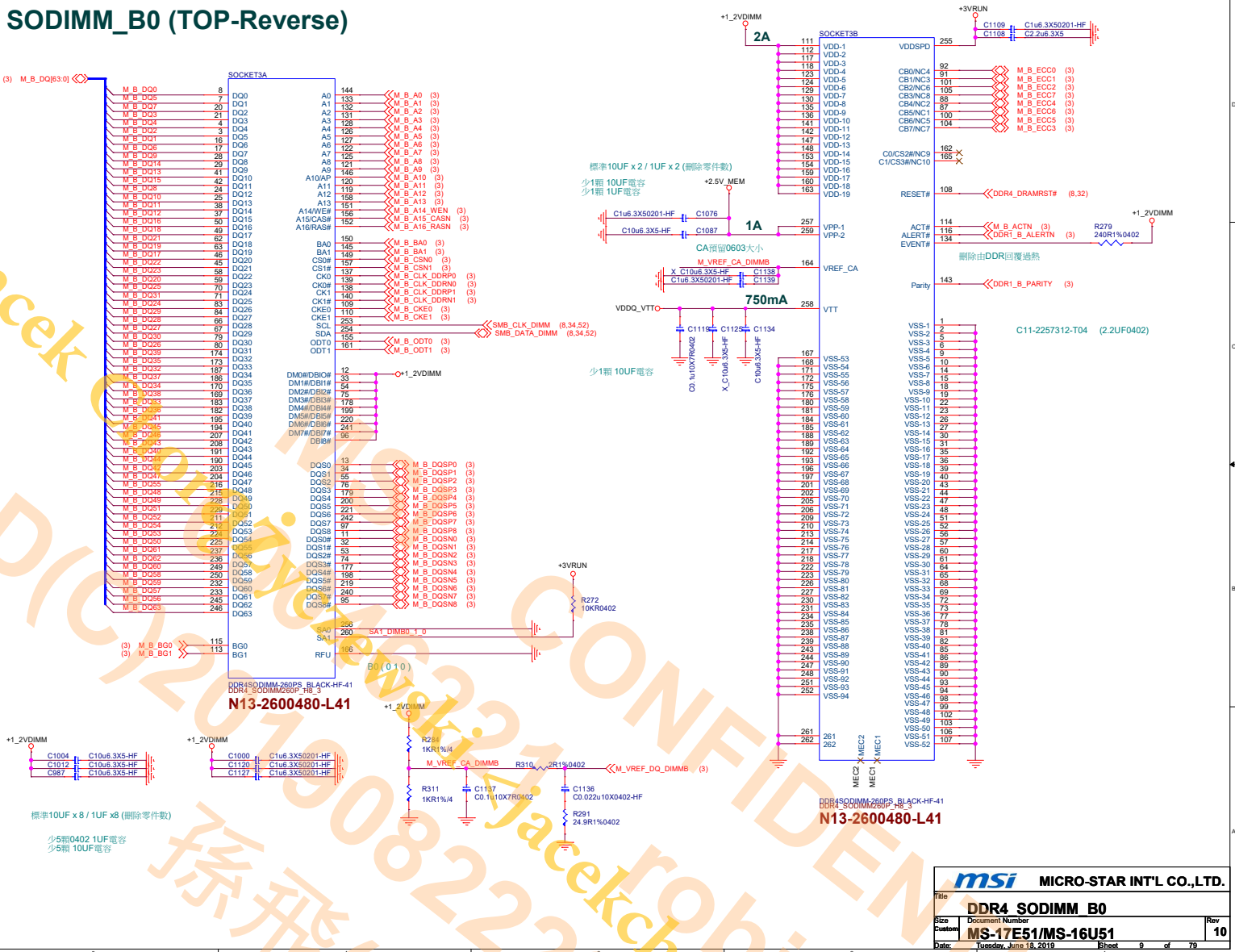


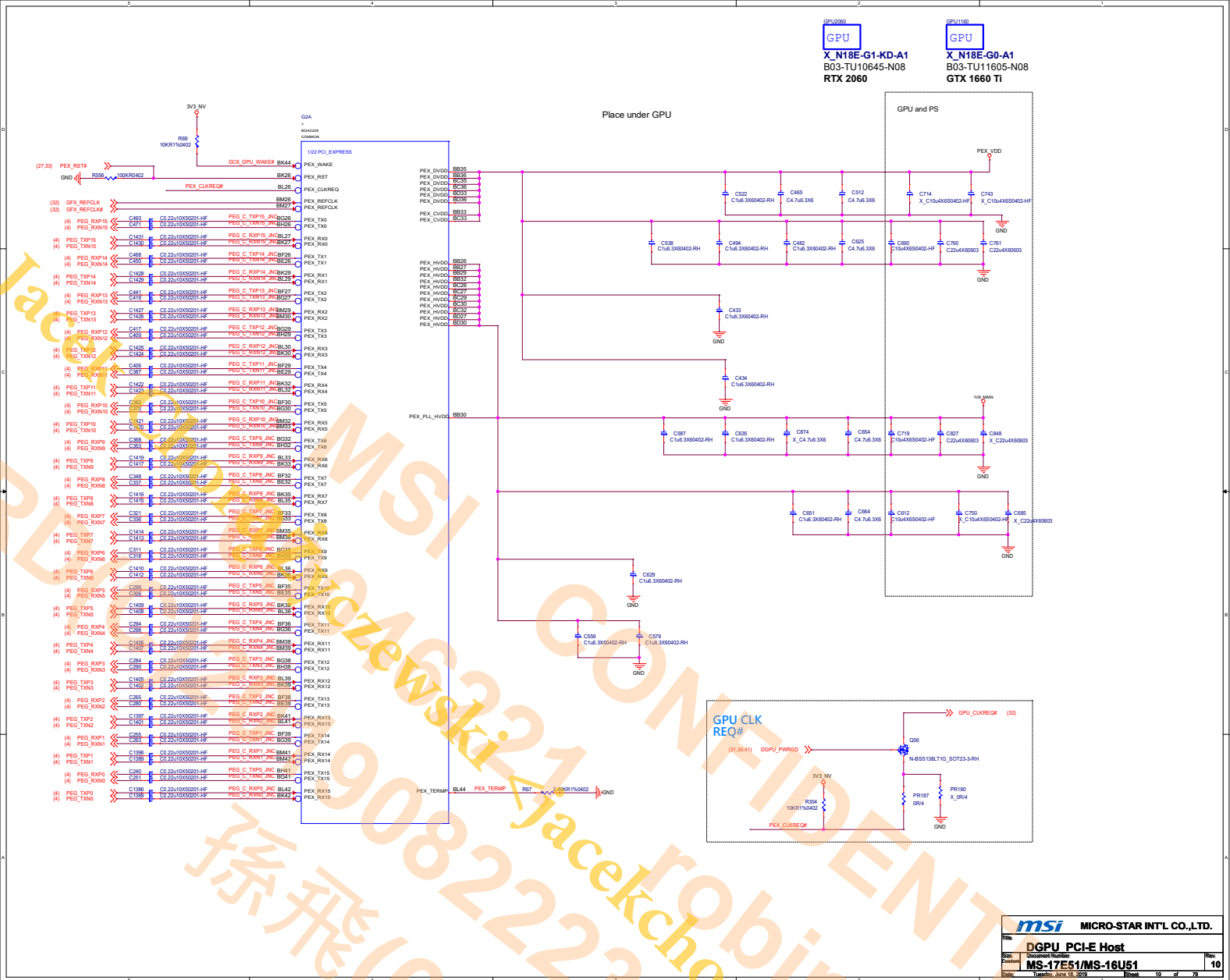


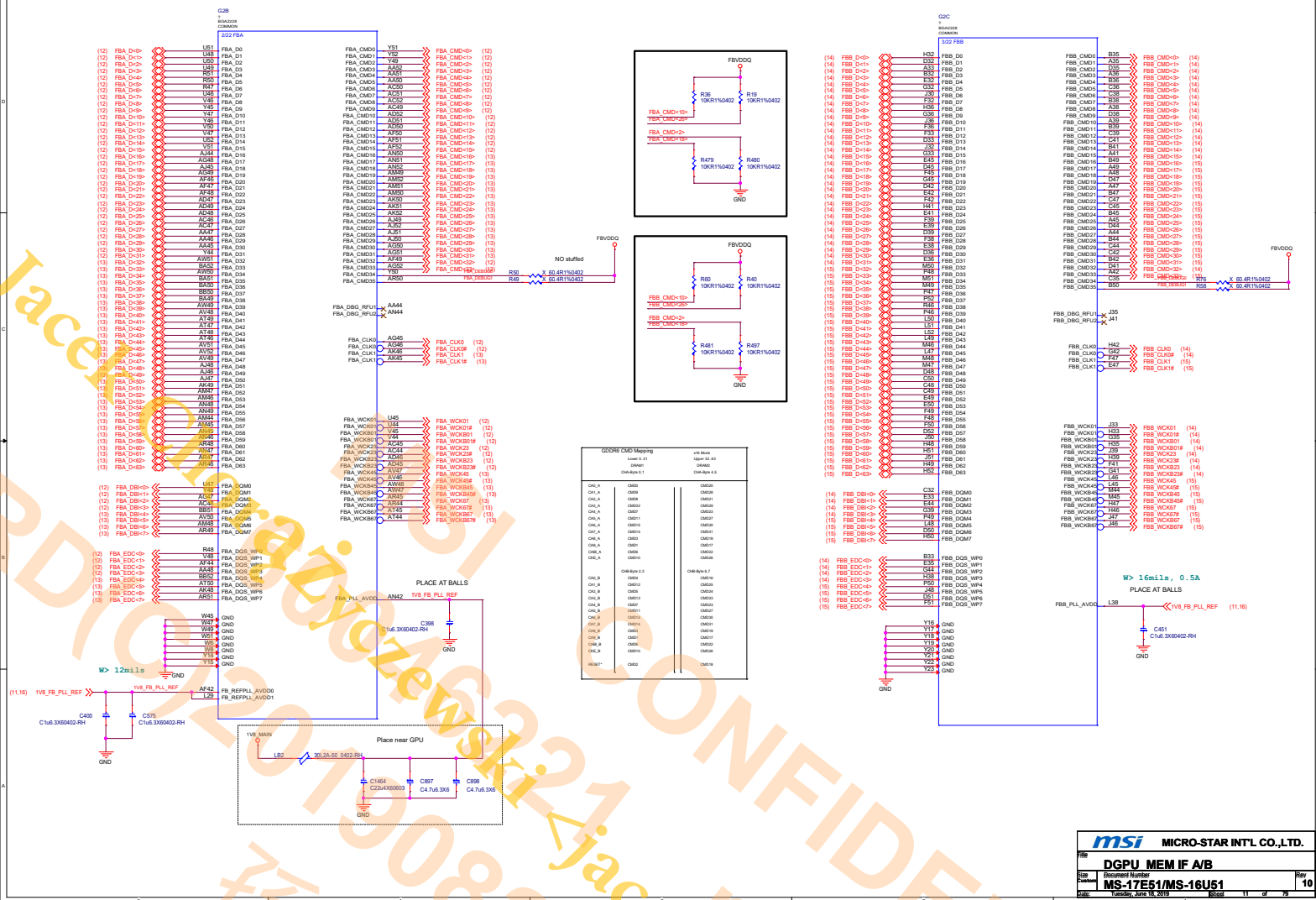


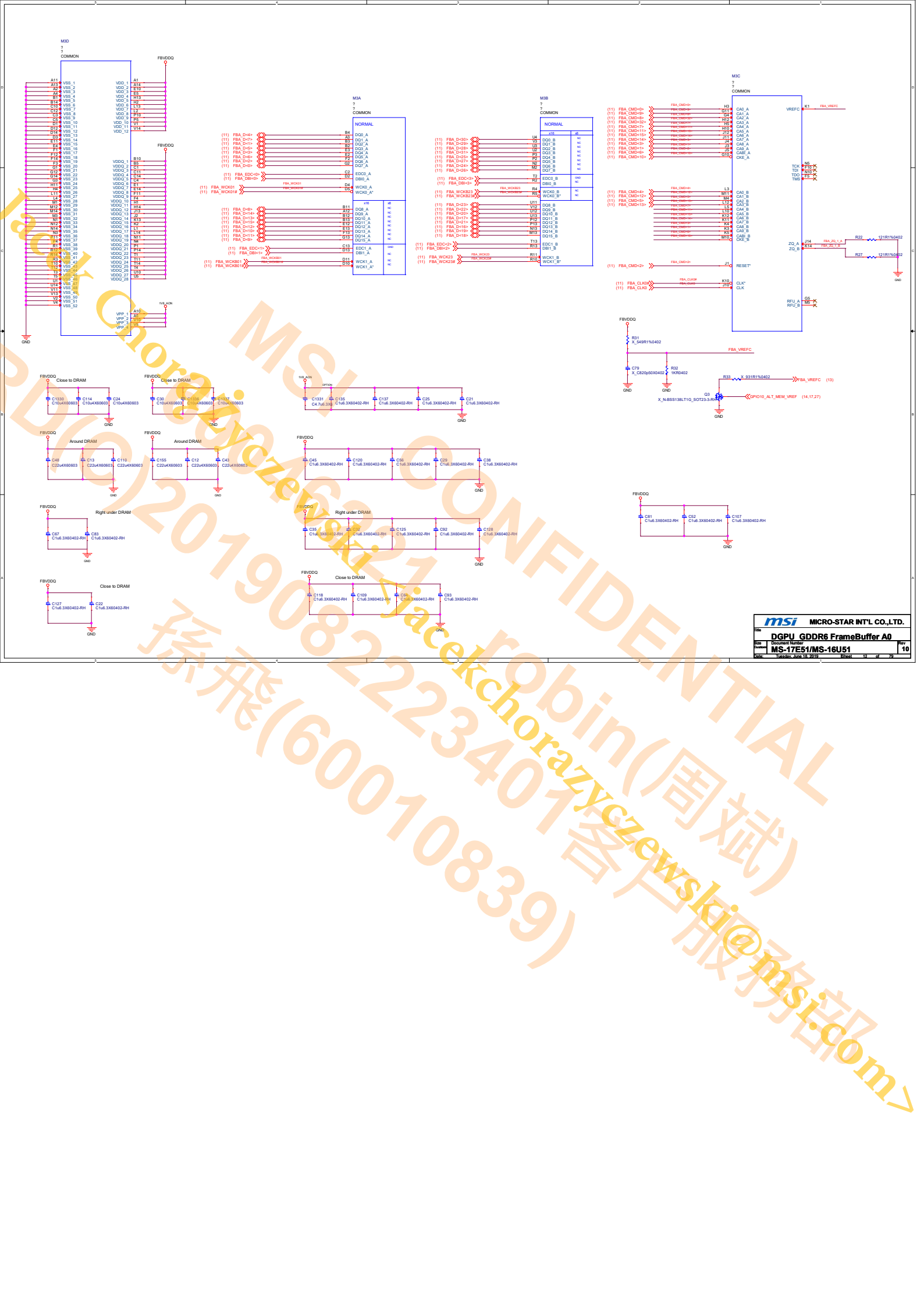


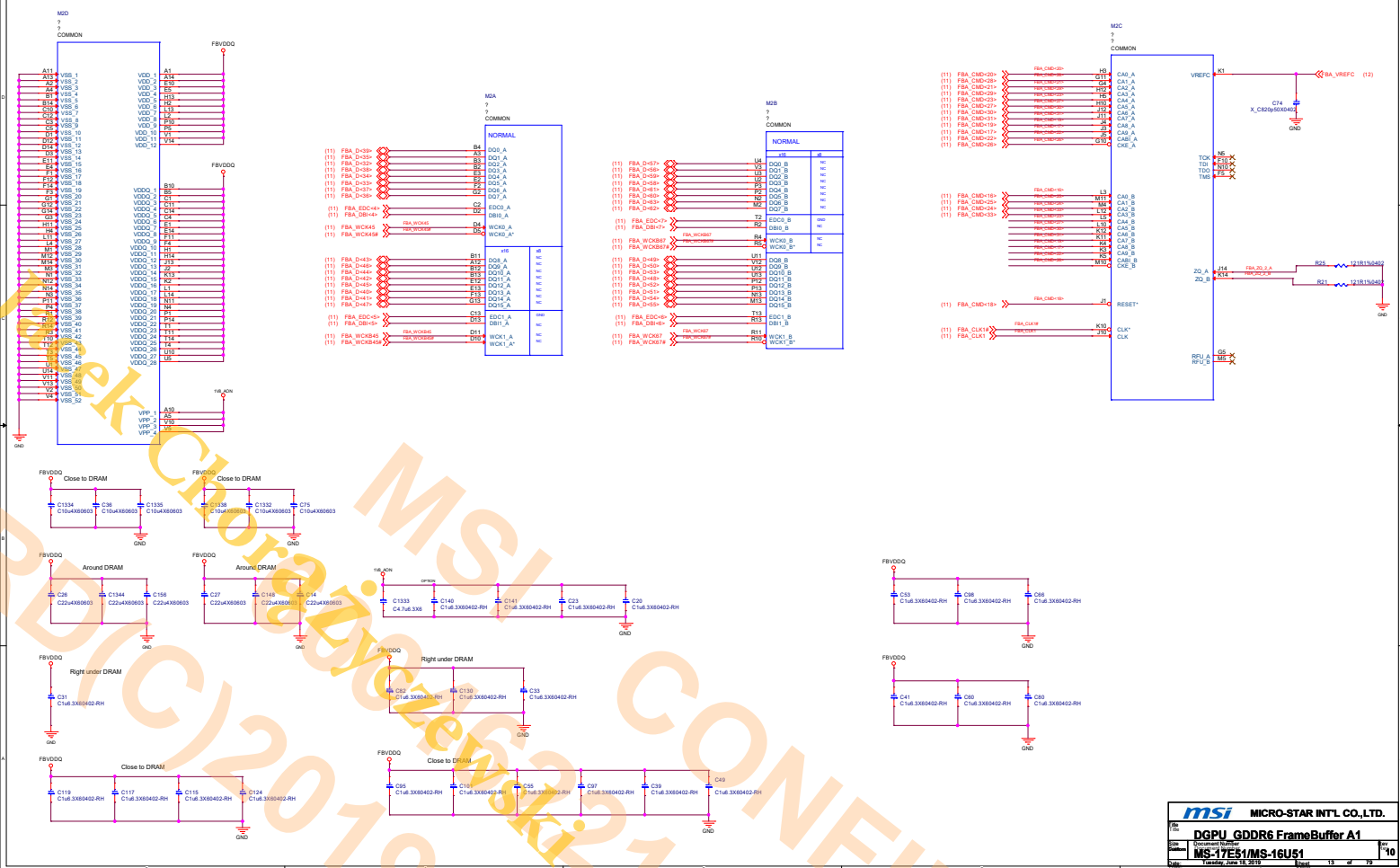
SODIMM_B0 (TOP-Reverse)

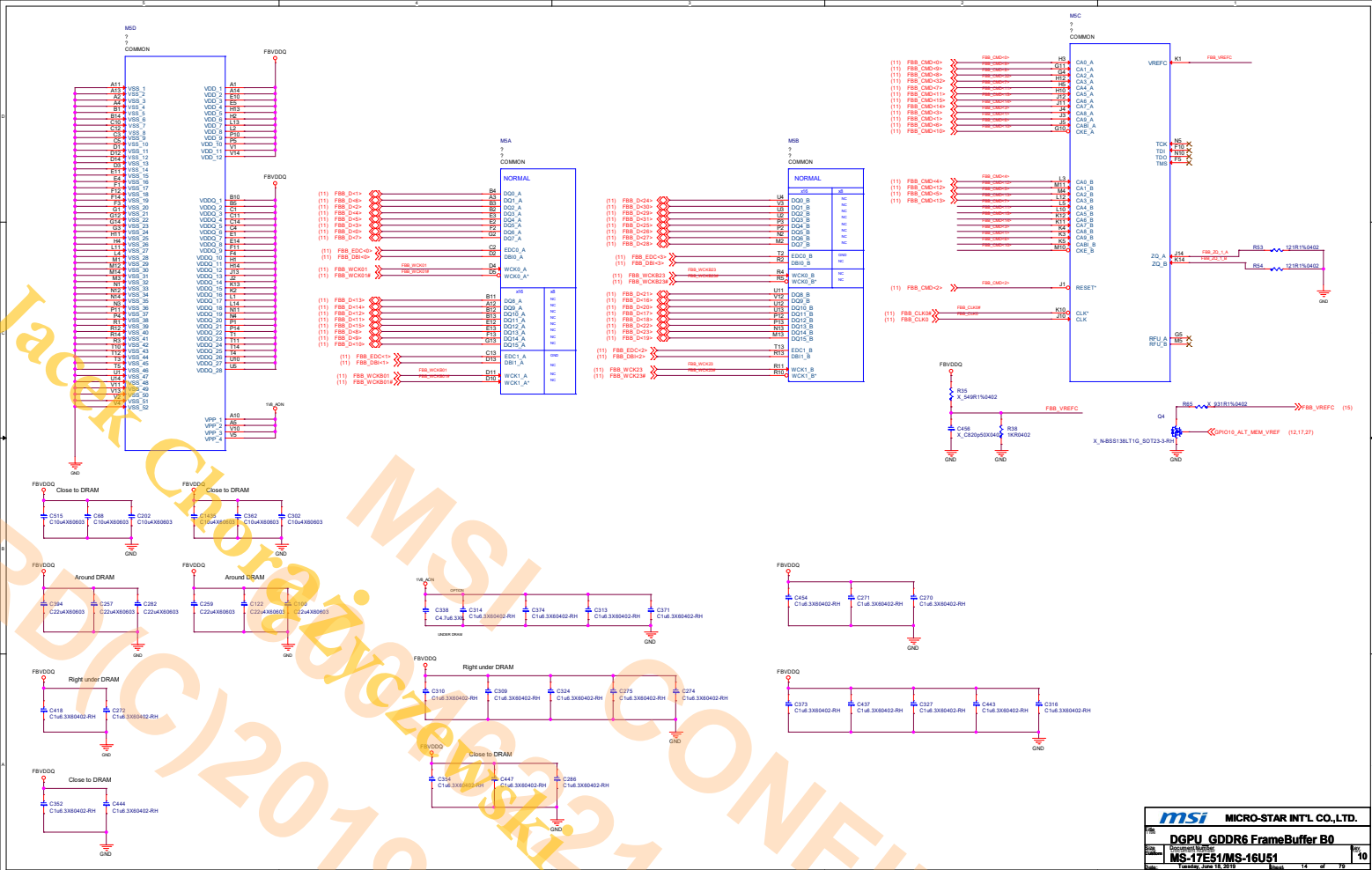


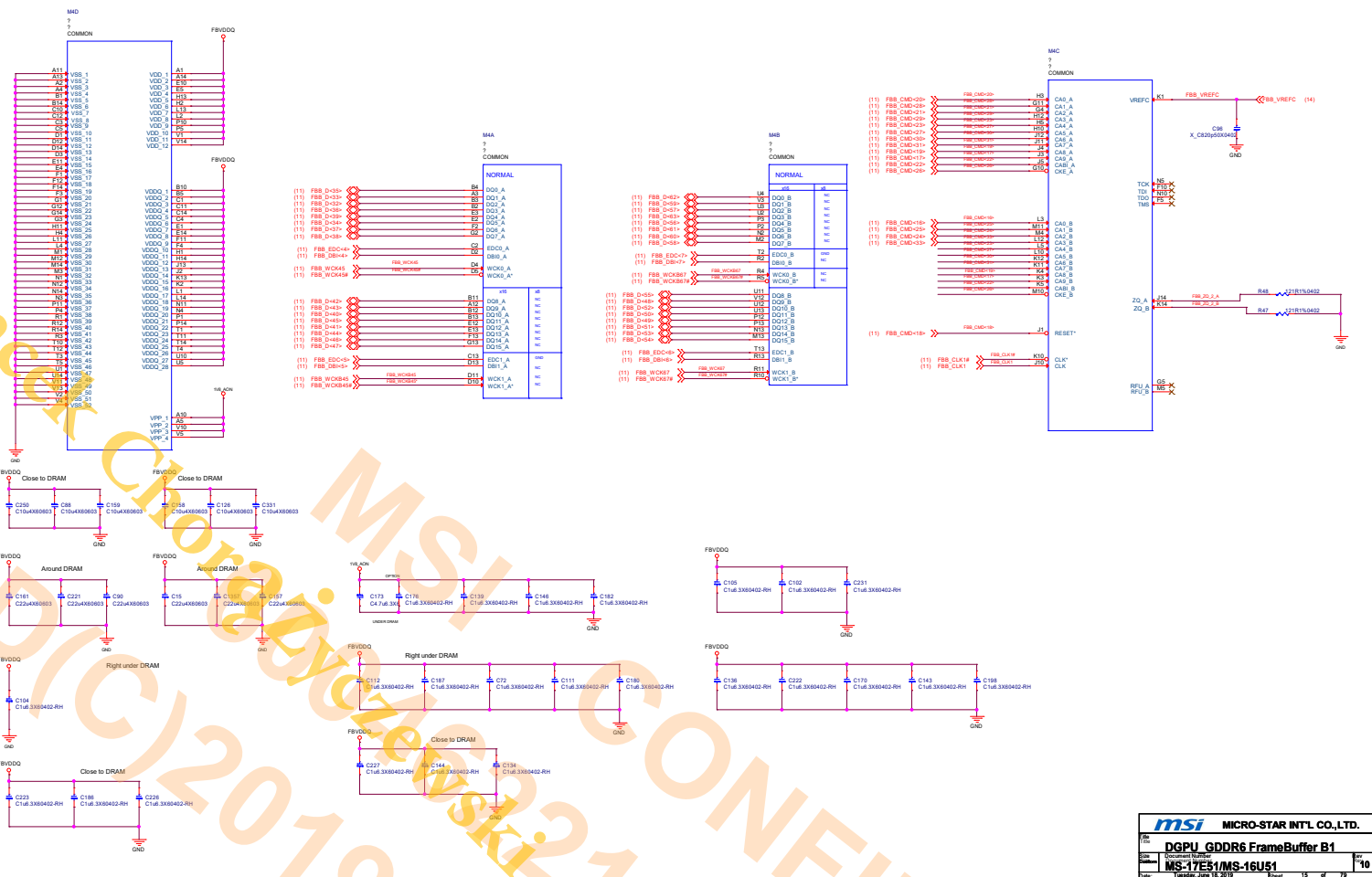


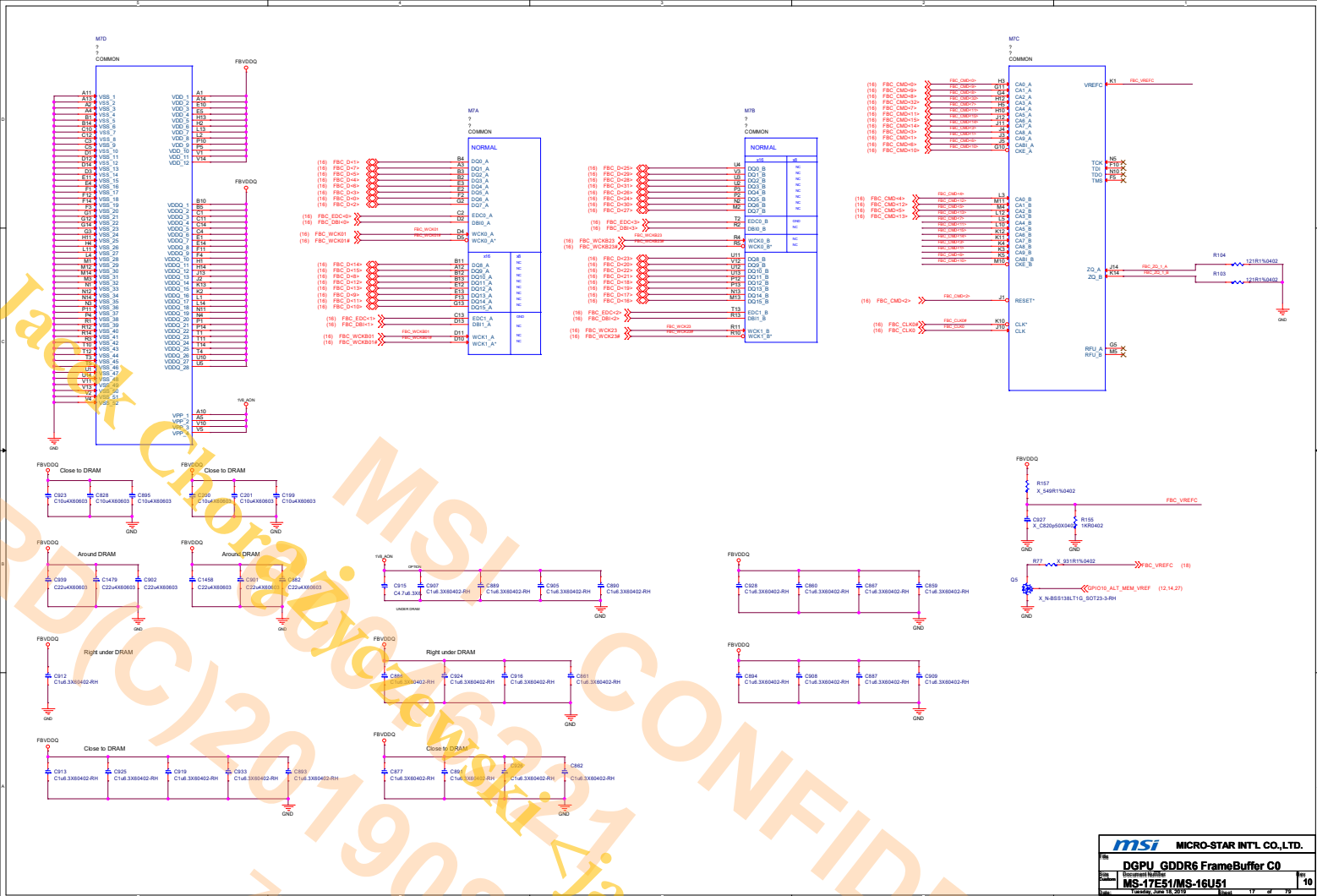


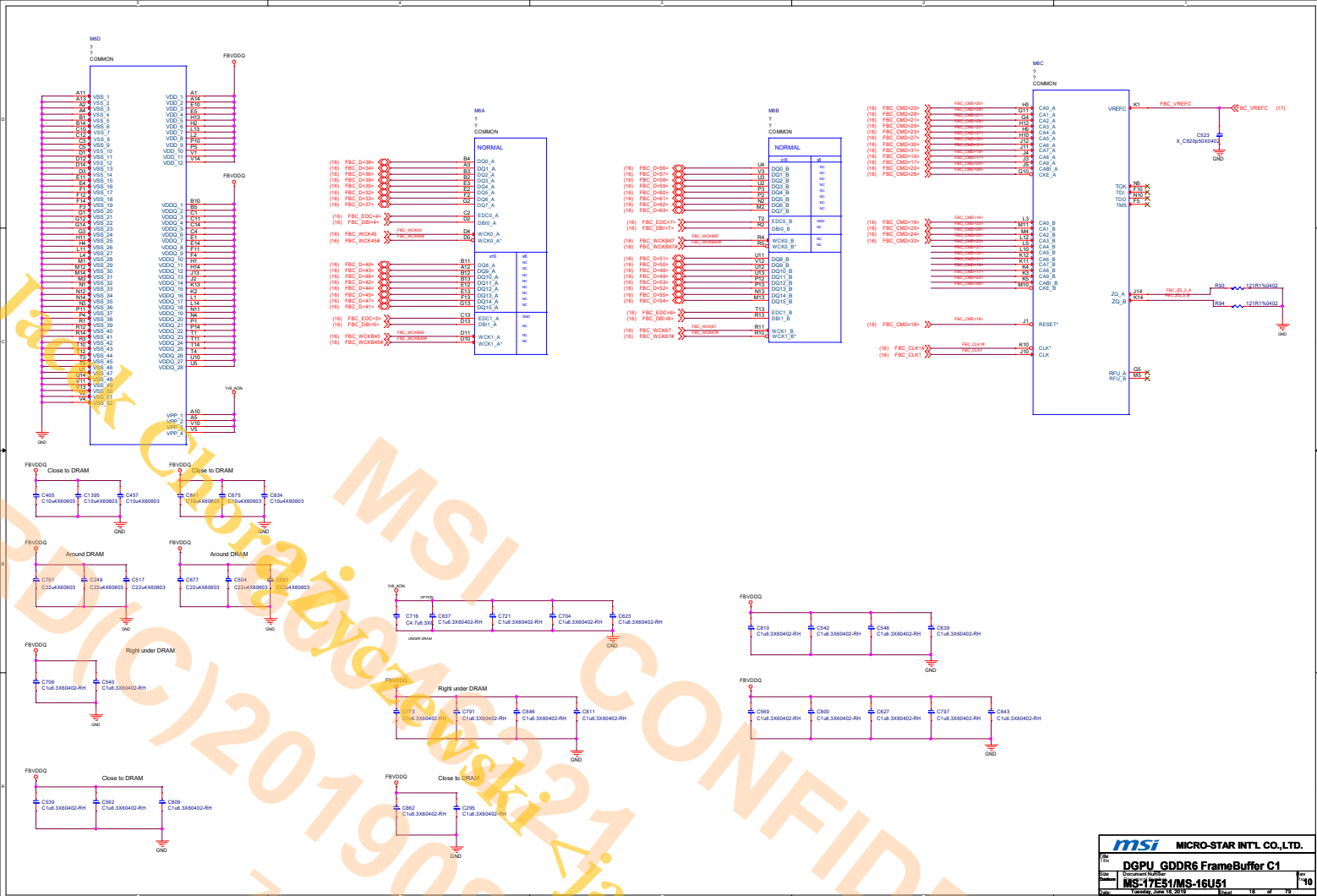


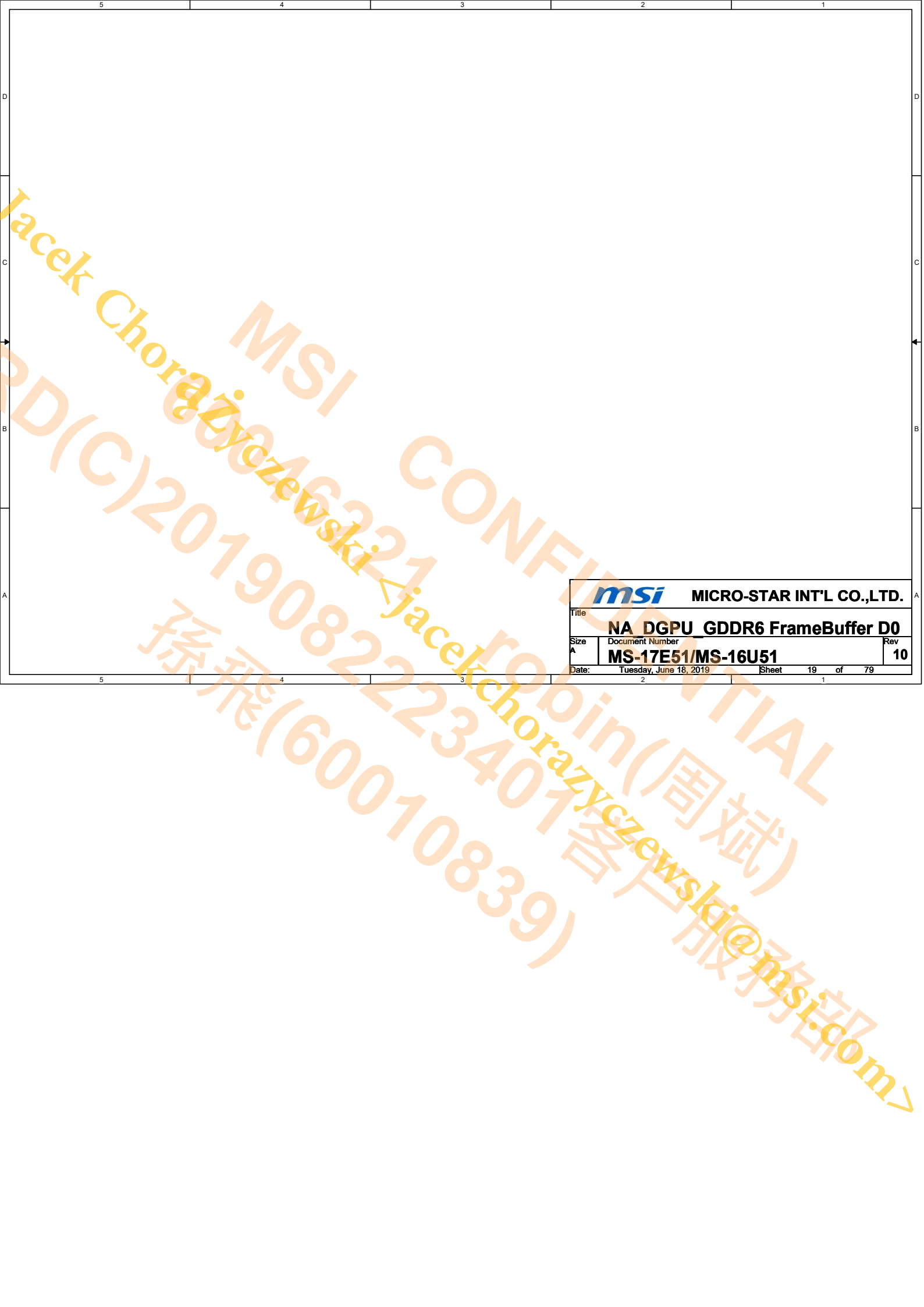














		MICRO-STAR INT'L CO.,LTD.	
Title			
NA DGPU GDDR6 FrameBuffer D0			
Size	Document Number		Rev
A	MS-17E51/MS-16U51		10
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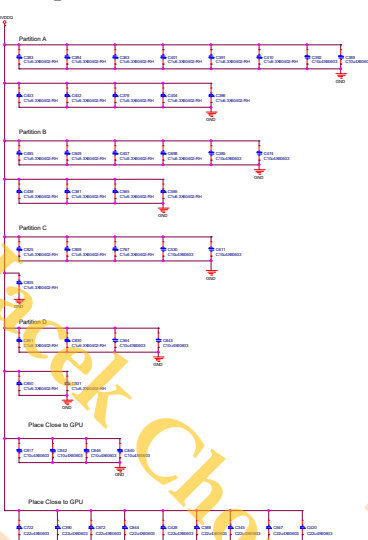
N18E-G1 stuff off.

 MICRO-STAR INT'L CO.,LTD.		
Title		
NA DGPU_GDDR6 FrameBuffer D1		
Size	Document Number	Rev
A	MS-17E51/MS-16U51	10
Date: Tuesday, June 18, 2019		
Sheet 20 of 79		

GPU PWR GND NCs



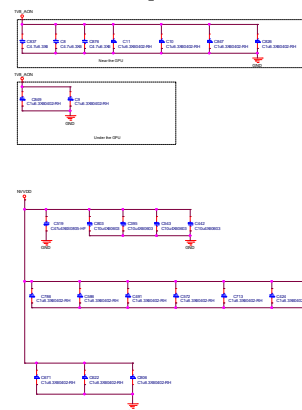
FBVDDQ_GPU



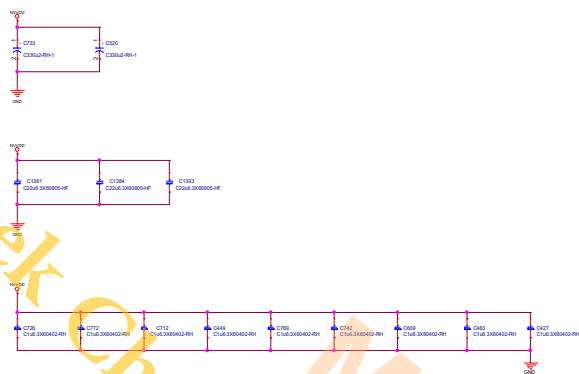
NVVDD

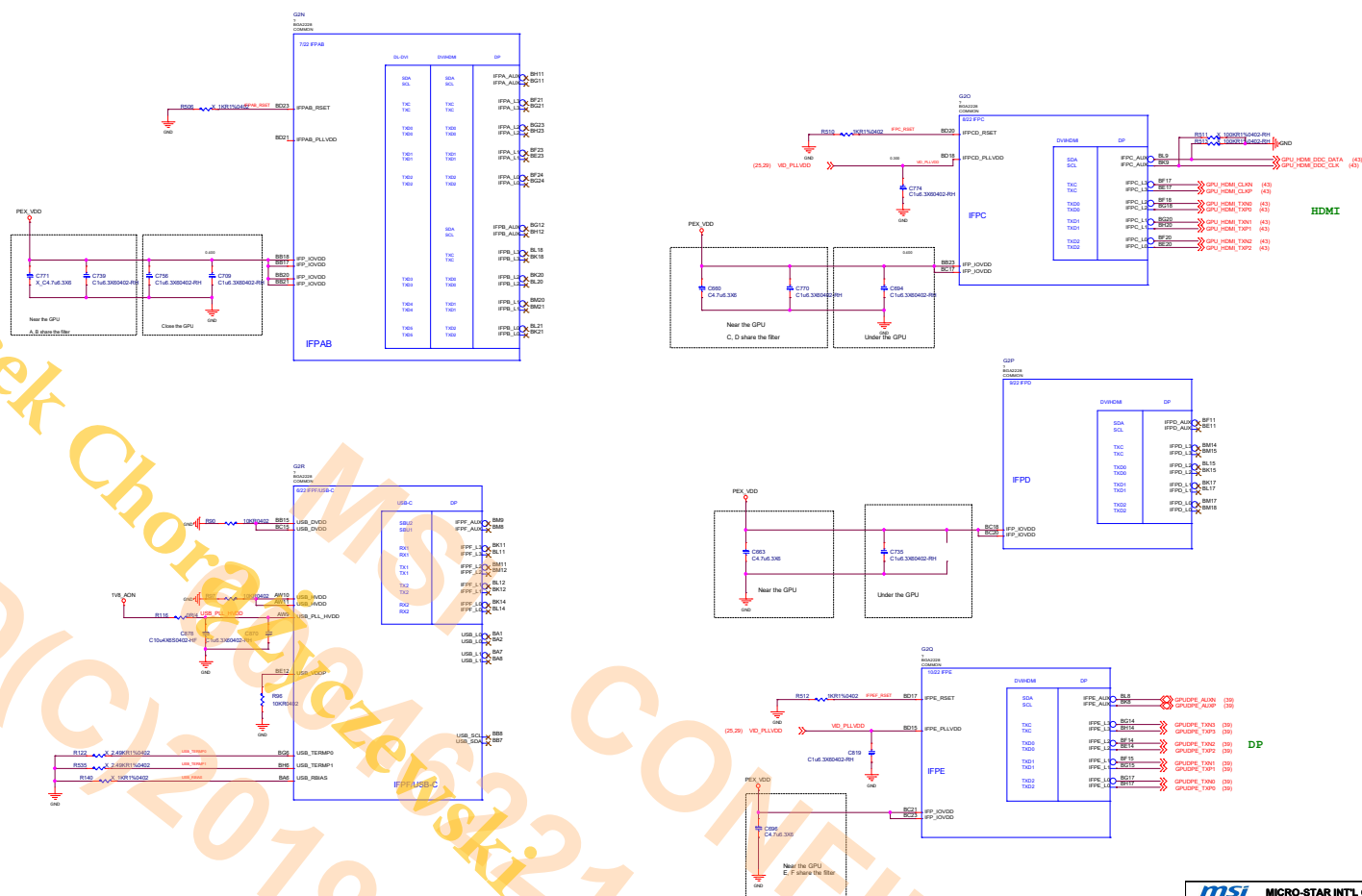


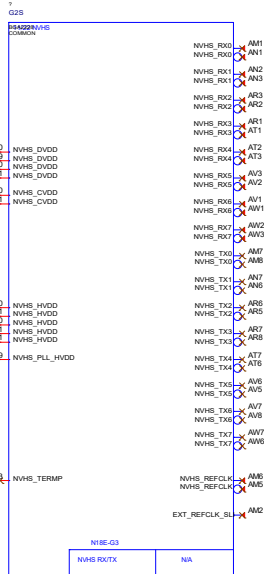
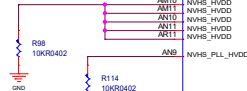
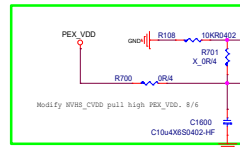
1V8_AON



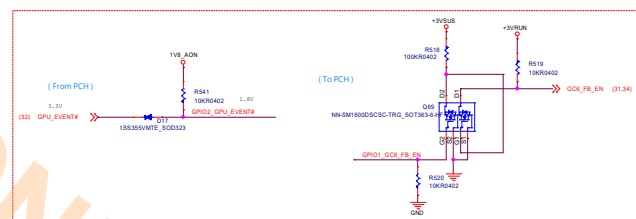
GPU Decoupling







msi MICRO-STAR INT'L CO.,LTD.	
GPU NVLink & Framelock	
Doc	Rev
MS-17E51/MS-16U51	10
Date: January, June 18, 2019	



Pin Name	Normal function	I/O	Functional Description	Recommended Default
GP100	NVDD_PFM_VID	0	PMU Output to control NVDD	5 to I/O PM output pull-up or pull-down
GP101	GC6_FB_EN	0	FB Enable for GC6 2.1	10K pull-up to I/O_AON
GP102	GPU_EVENTS	1	GPU wake signal for GC6 2.1	10K pull-up to I/O_AON
GP103	UNUSED	0		
GP104	I/O_MAIN_EN	0	GPU POWER Selection for GC6 2.1	10K pull-up to I/O_AON
GP105	FRAME_LOCK	1	Active Low Frame Lock	10K pull-up to I/O_AON
GP106	VIDEO_PSI	0	Phase shedding	10K pull-up to I/O_AON
GP107	LCD_IL_PWM	0	LCD Panel Backlight PWM	10K pull-up to I/O_AON
GP108	MEM_VDD_CTL	0	Memory Voltage Control	10K pull-up to I/O_AON
GP109	TEMPER_ALERT	I/O	Active Low Thermal Alert	10K pull-up to I/O_AON
GP110	MEM_VREF_CTL	0	Memory VREF Control	10K pull-up to I/O_AON
GP111	LCD_VCC	0	Panel Power Enable	10K pull-up to I/O_AON
GP112	PWR_LEVEL	1	AC power detect or power supply overvoltage input	10K pull-up to I/O_AON
GP113	UNUSED	0		
GP114	RPO_IPFA	1	Not Plug Detect for IPFA	10K pull-up to I/O_AON
GP115	RPO_IPFB	1	Not Plug Detect for IPFB	10K pull-up to I/O_AON
GP116	UNUSED	0		
GP117	RPO_IPFD	1	Not Plug Detect for IPFD	10K pull-up to I/O_AON
GP118	RPO_IPFF	1	Not Plug Detect for IPFF	10K pull-up to I/O_AON
GP119	Reserved	0		
Pin Name				
GP120	MS_F0CE	0		10K pull-down
GP121	LCD_BLEN	0	LCD Panel Backlight Enable	100K pull-down
GP122	SWAPPY_IN	0		2.2K pull-up to I/O_AON
GP123	RASTER_SYNC1	0		100K pull-down
GP124	NOT PLUG DETECT FOR RPO OR DONGLE SET	1	Not Plug Detect for RPO or USB	10K pull-up to I/O_AON
GP125	FEVDD_PSI	0		
GP126	FF_F0CE	0		10K pull-down
GP127	RPO_IPFC	1	Not Plug Detect for IPFC	10K pull-up to I/O_AON
GP128	I/O_IL/ACC_MUX_SEL	0		10K pull-up
GP129	I/O_IL_SW	1		10K pull-up
GP130	UNUSED	0		

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

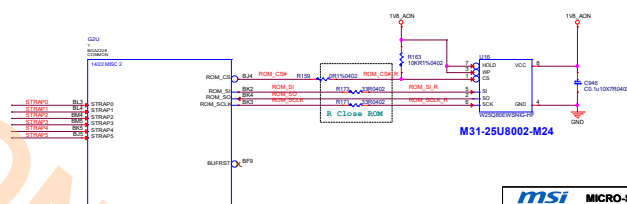
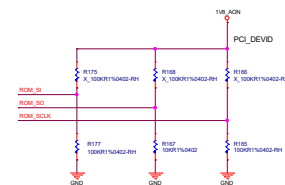
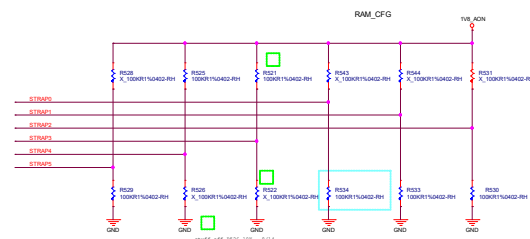
STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	L	H	00001	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

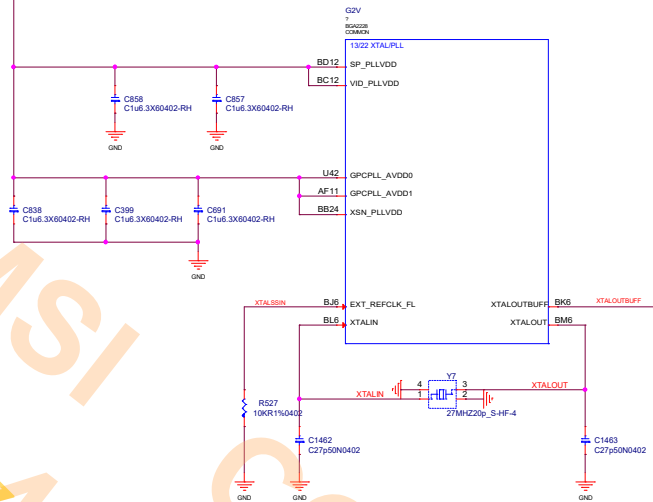
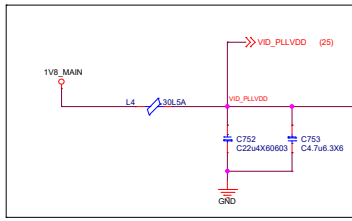
RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Hynix
00111	16Gb	256-bit	Samsung
01000	16Gb	256-bit	Micron

ROM_SO	ROM_S1	ROM_S0LK	DUMMY(2:0)_FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCI_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	H	L	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL
1:PCI_CFG LOW POWER
0:PCI_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE





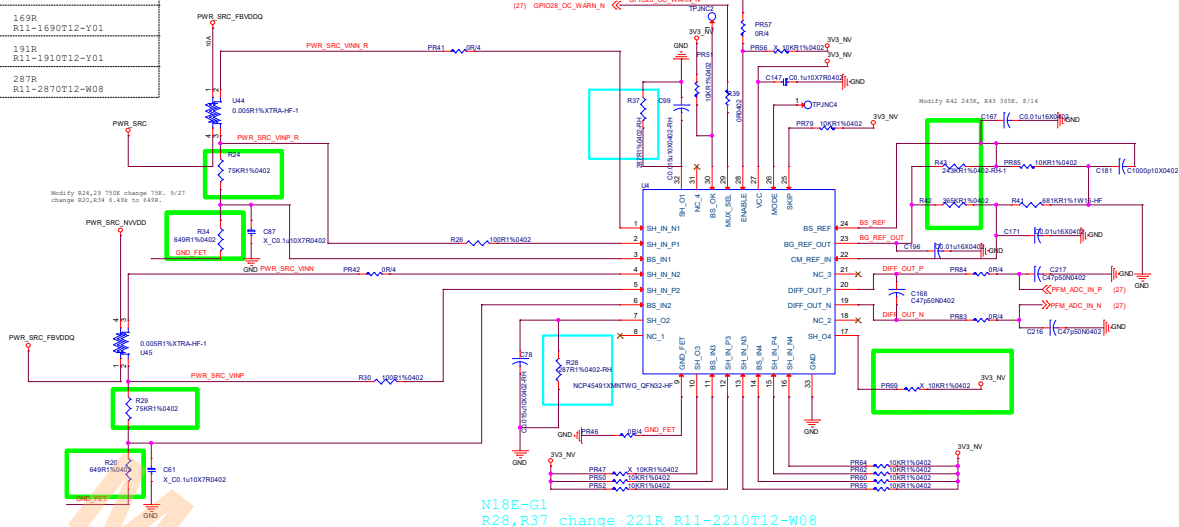
SmartFan Strap Table

XTALOUTBUFF STRAP VALUE	Voltage	Inverted SmartFan PWM %
0	0V	GPIO DISABLED
1	0.9V	33% PWM
3	1.0V	66% PWM

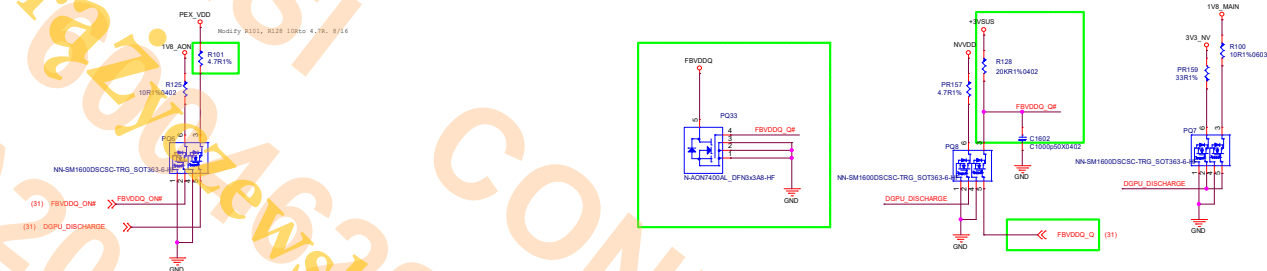
msi MICRO-STAR INT'L CO.,LTD.	
Title: DGPU MIO & XTAL	
Step: 1	Document Number: MS-17E51/MS-16U51
Date: Tuesday, June 18, 2019	Sheet: 29 of 79

DGPU_Power Control

TGP	SKU	R24,R29	R34,R20	C87,C61 先不上件	R37,R28
150W+	G3	75K	649R	InF	169R R11-1690T12-Y01
115W to 150W	G2	75K	649R	InF	191R R11-1910T12-Y01
75W to 95W	G1	75K	649R	InF	287R R11-2870T12-W08

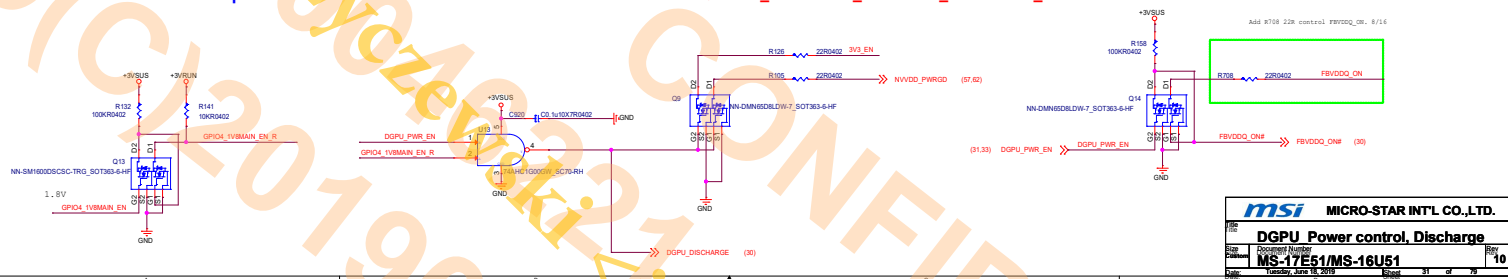


Discharge

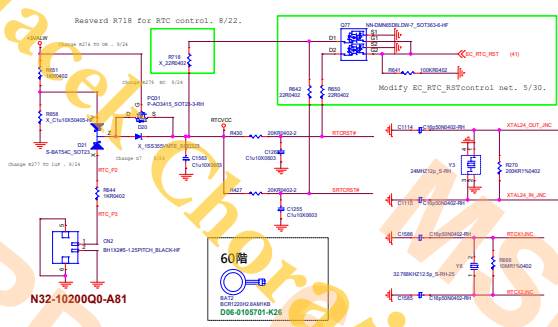
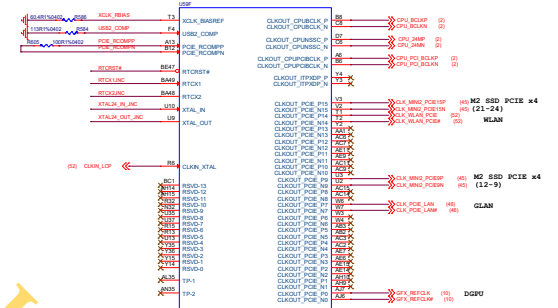


msi MICRO-STAR INT'L CO., LTD.	
DGPU Power Control	
Part Number	MS-17E51/MS-16U51
Date	Monday, June 18, 2019
Page	10 of 10

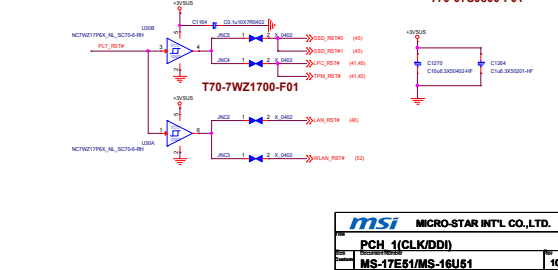
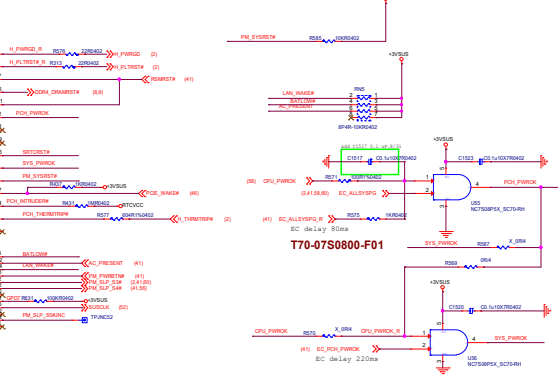
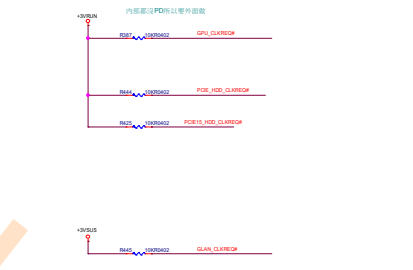
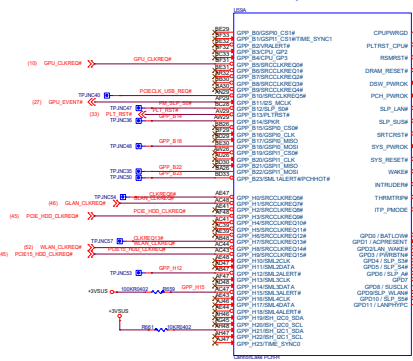
Power on = 1V8_AON -> 1V8_MAIN -> 3V3_NV -> NVVDD -> PEX_VDD -> FBVDDQ -> DGPUPWRGD



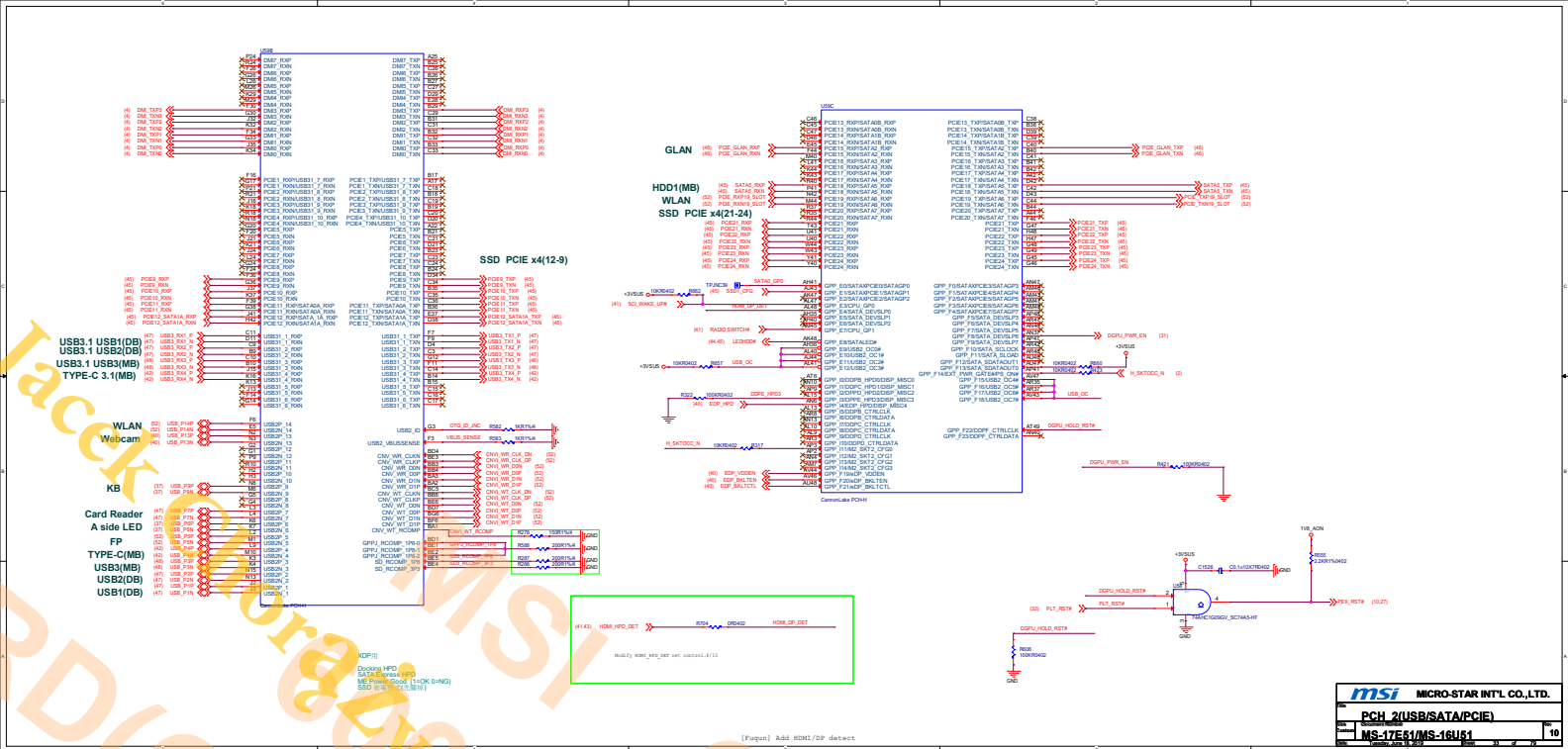
HM370 (RTC/PCIE_Clock/Clock/RSVD)

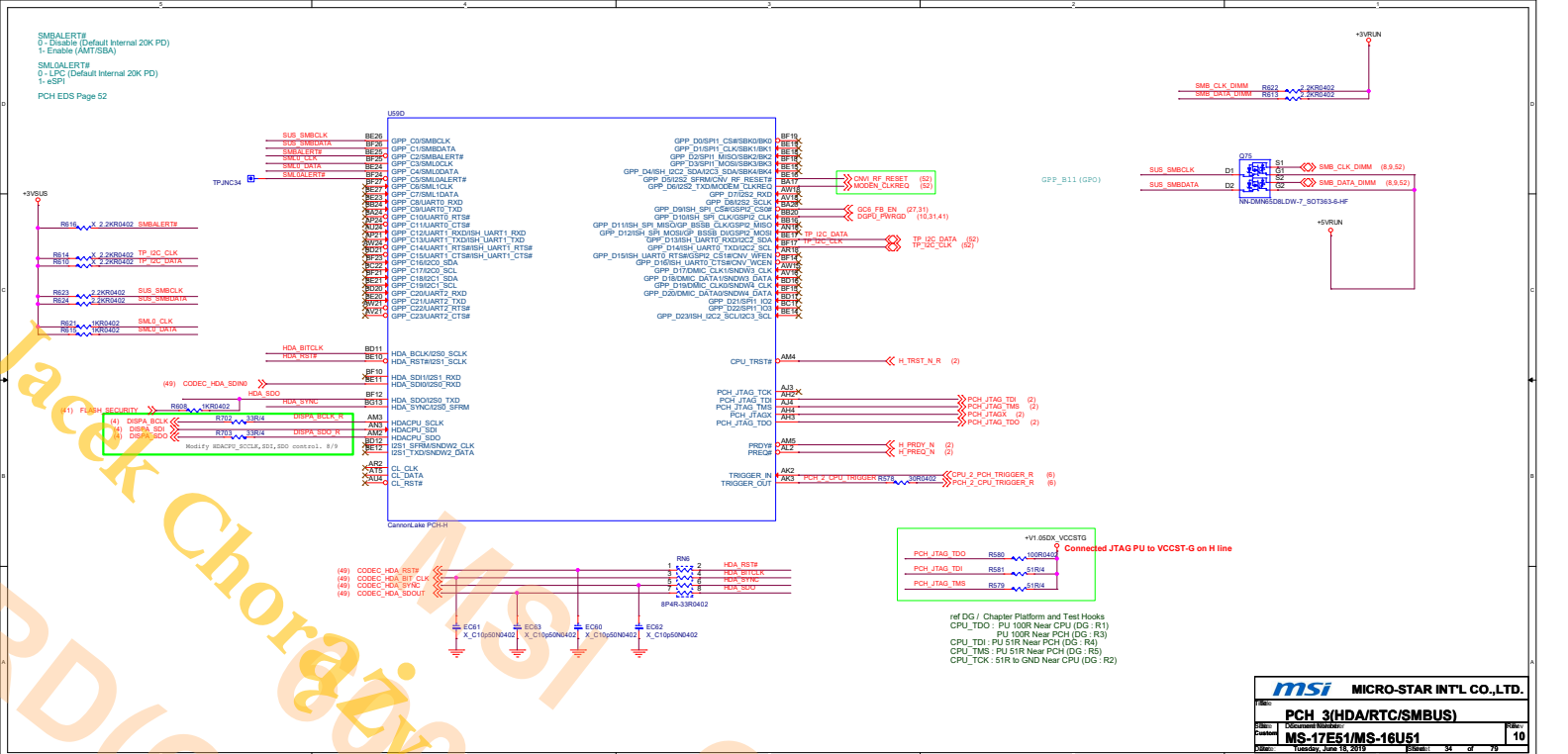


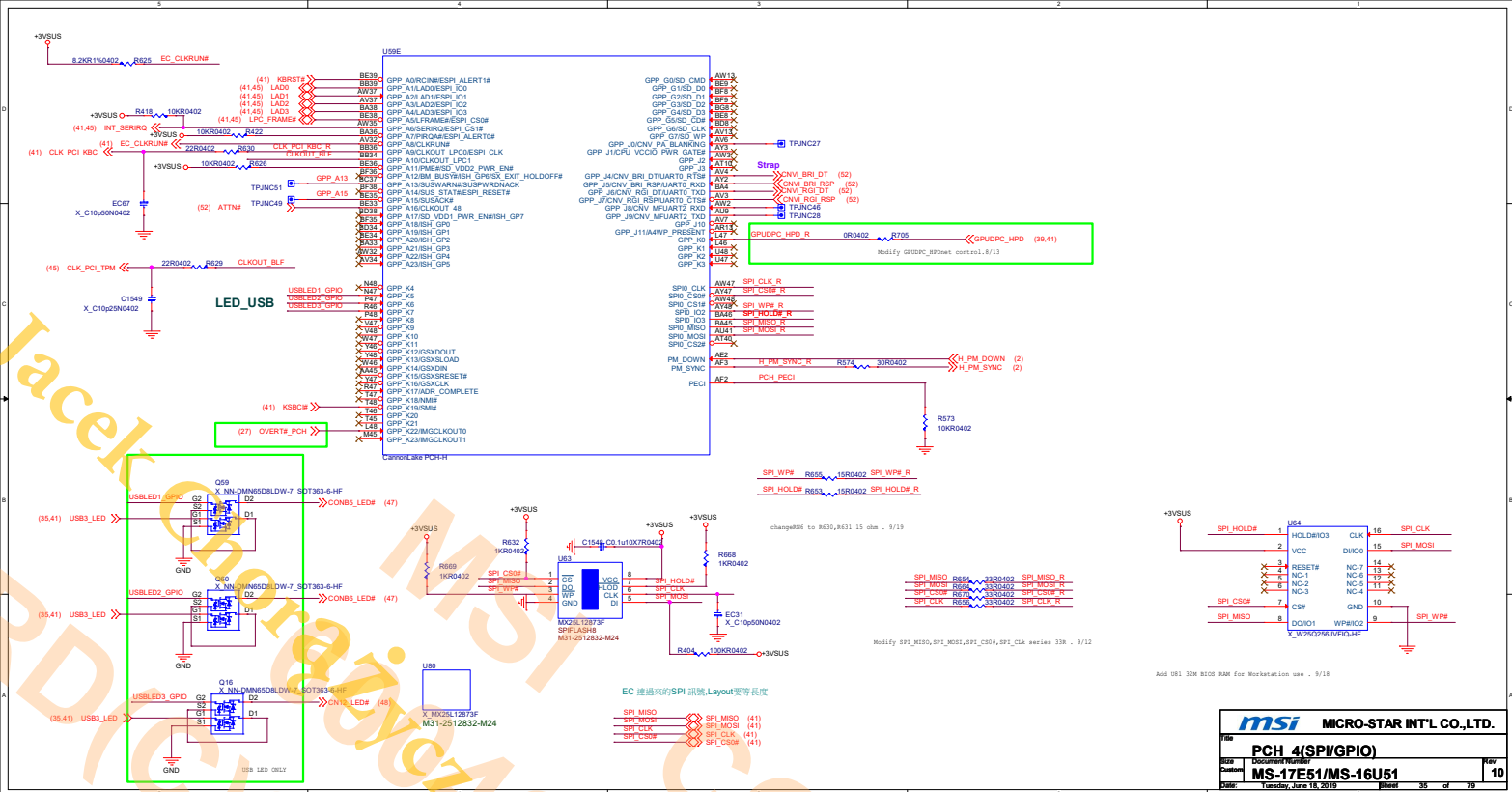
HM370 (CLKREQ/ACPI)



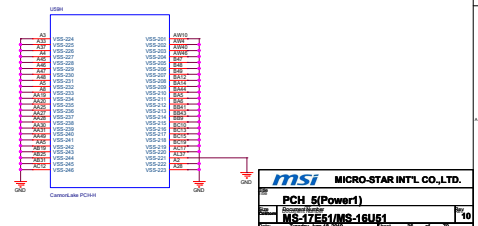
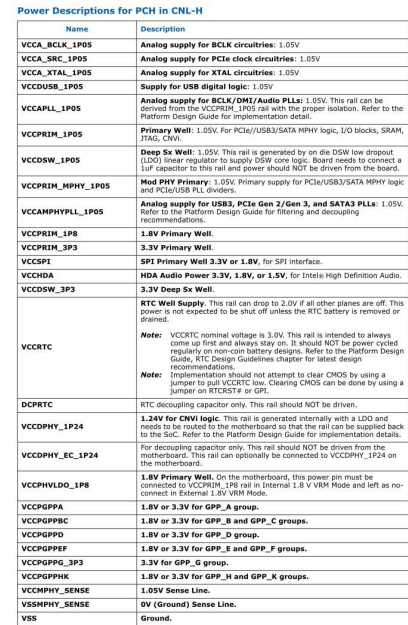
msi MICRO-STAR INT'L CO.,LTD.	
PCH 1(CLK/DDI)	
MS-17E61/MS-16U61	
10	



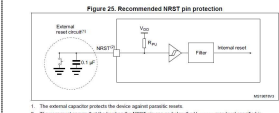
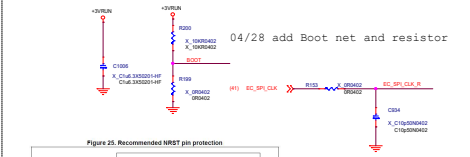
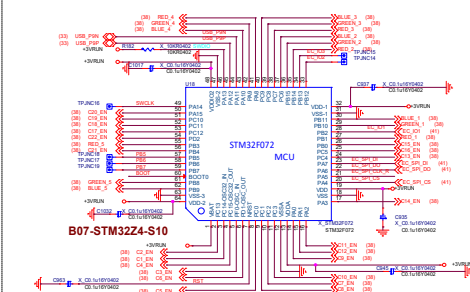




ref DG / Table 50-6 Decoupling Requirements

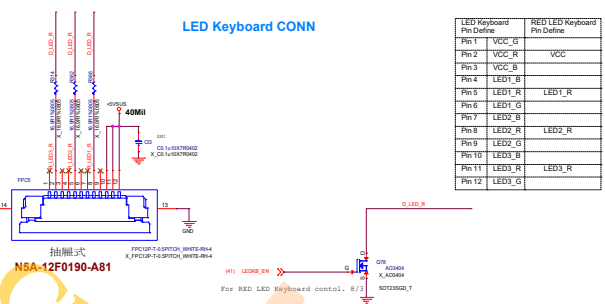


LED STM32F072 Controller

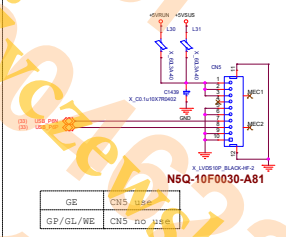


1. The external resistor protects the device against possible faults.
2. The capacitor protects the device against possible faults.
3. The capacitor protects the device against possible faults.

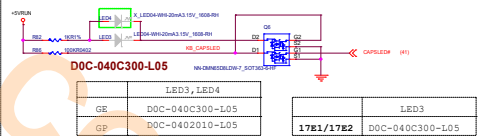
LED Keyboard CONN



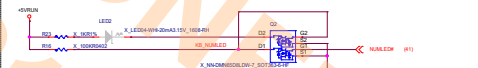
side LED

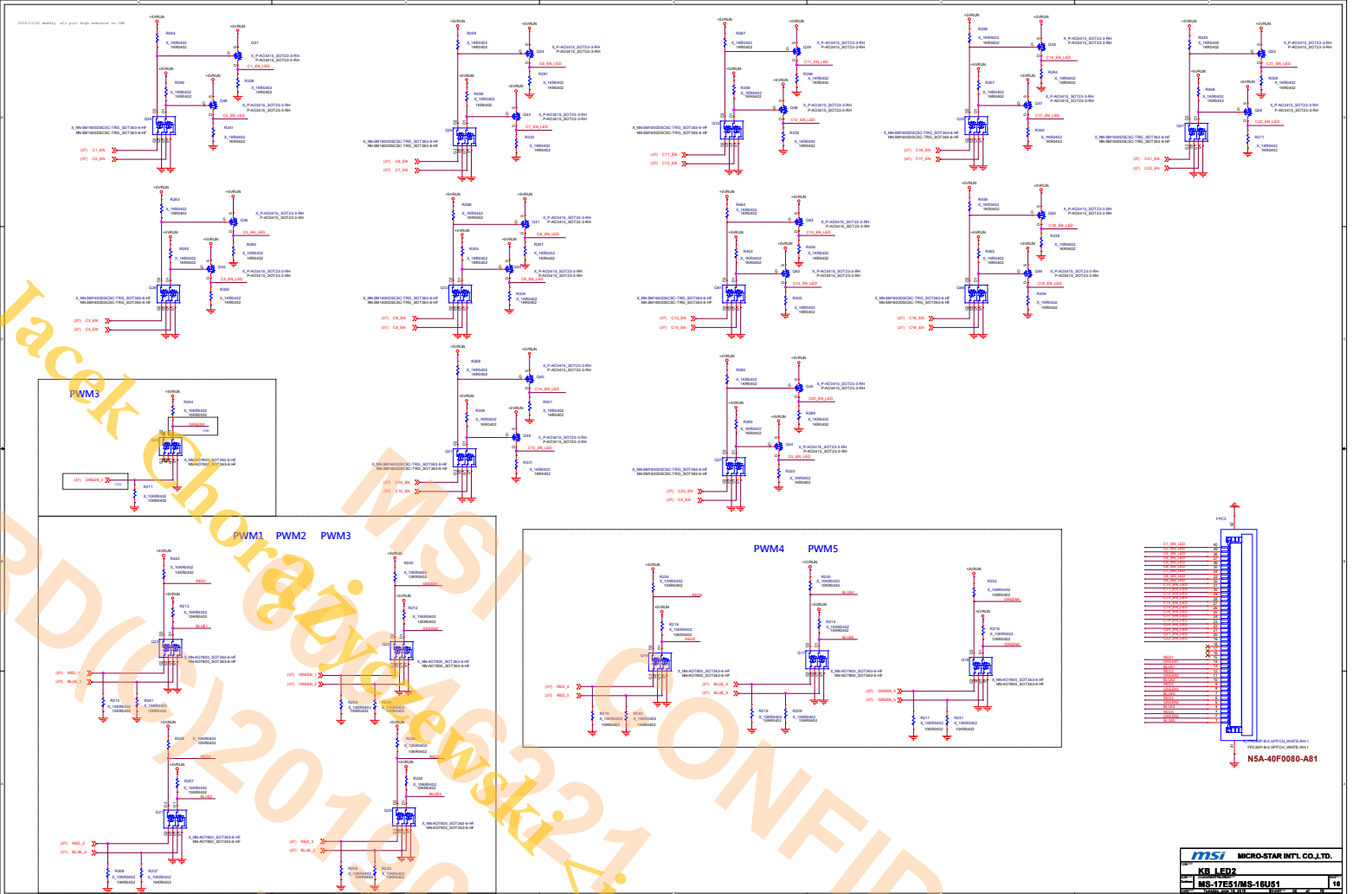


CAPSLED Add LED4 for17"

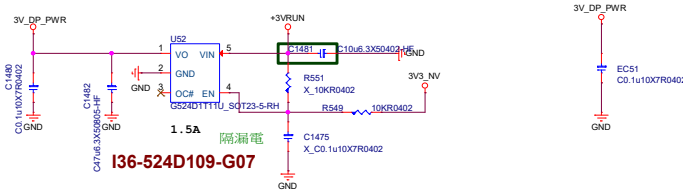


NUMLED

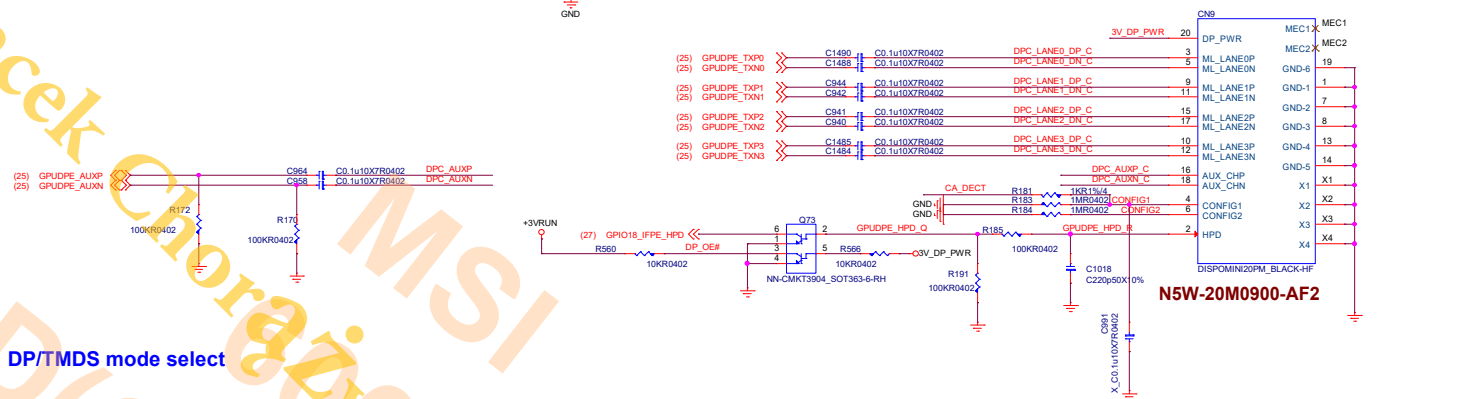




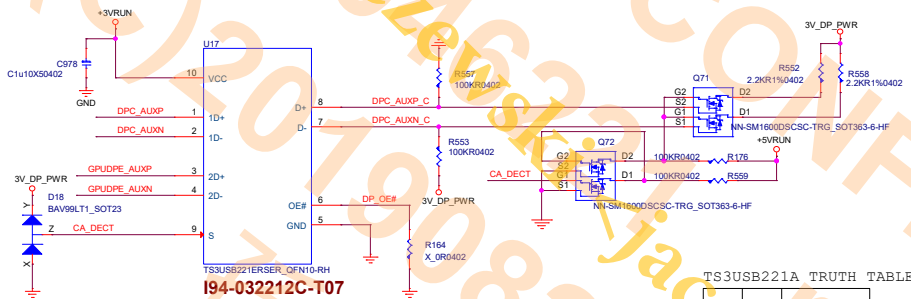
The preset trip limit must not exceed 3A at the Upstream device connector DP_PWR pin and 1.5A at the Downstream device connector DP_PWR pin.



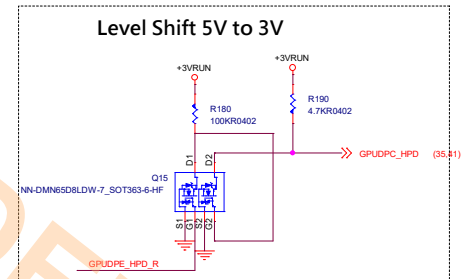
Display Port



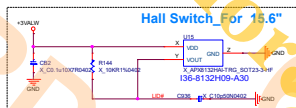
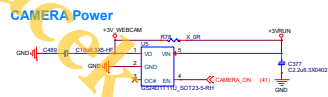
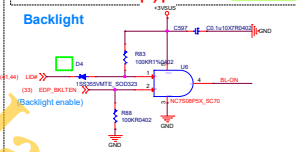
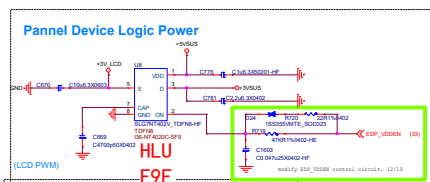
DP/TMDS mode select



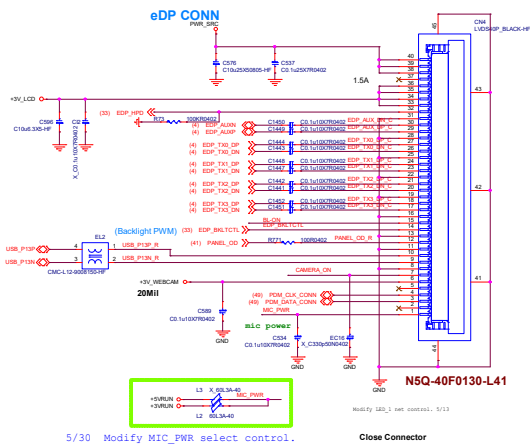
Level Shift 5V to 3V



S	OE#	FUNCTION
X	H	Disconnect
L	L	D = 1D
H	L	D = 2D



CAMERA



5/30 Modify MIC_PWR select control.



LCD Module Pin Define FOR FULL HD PANEL

Pin No	Symbol	Description
1	Vcom_SDA	Vcom IIC SDA
2	H_GND	High Speed Ground
3	LAN1_N	Complement Signal-Lane 1
4	LAN1_P	True Signal-Main Lane 1
5	H_GND	High Speed Ground
6	LAN0_N	Complement Signal-Lane 0
7	LAN0_P	True Signal-Main Lane 0
8	H_GND	High Speed Ground
9	AUX+	True Signal-Auxiliary Channel
10	AUX-	Complement Signal-Auxiliary Channel
11	H_GND	High Speed Ground
12	LCD_VDD	Power Supply +3.3 V (typical)
13	LCD_VDD	Power Supply +3.3 V (typical)
14	NC	No Connection (Reserved for CMI test)
15	H_GND	Ground
16	H_GND	Ground
17	HPD	Hot Plug Detect
18	BL_GND	BL Ground
19	BL_GND	BL Ground
20	BL_GND	BL Ground
21	BL_GND	BL Ground
22	BL_EN	BL Enable Signal of LED Converter
23	BL_PWM	PWM Dimming Control Signal of LED Converter
24	Vcom_SCL	Vcom IIC SCL
25	NC	No Connection (Reserved)
26	LED_VDD	BL Power
27	LED_VDD	BL Power
28	LED_VDD	BL Power
29	LED_VDD	BL Power
30	OD_EN	OD Enable Signal of YCON

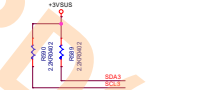
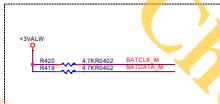
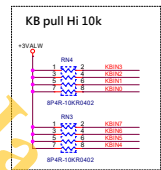
LCD Module Pin Define FOR WQHD PANEL

Pin No	Symbol	Description
1	NC	Reserved for LCD manufacturer's use
2	H_GND	High Speed Ground
3	Lane3_N	Complement Signal Link Lane 3
4	Lane3_P	True Signal Link Lane 3
5	H_GND	High Speed Ground
6	Lane2_N	Complement Signal Link Lane 2
7	Lane2_P	True Signal Link Lane 2
8	H_GND	High Speed Ground
9	Lane1_N	Complement Signal Link Lane 1
10	Lane1_P	True Signal Link Lane 1
11	H_GND	High Speed Ground
12	Lane0_N	Complement Signal Link Lane 0
13	Lane0_P	True Signal Link Lane 0
14	H_GND	High Speed Ground
15	AUX_CH_P	True Signal Auxiliary Channel
16	AUX_CH_N	Complement Signal Auxiliary Channel
17	H_GND	High Speed Ground
18	VDD	LCD logic and driver power(3.3V)
19	VDD	LCD logic and driver power(3.3V)
20	VDD	LCD logic and driver power(3.3V)
21	VDD	LCD logic and driver power(3.3V)
22	BIST	BIST (pattern selection L : Disable (default), H : Enable)
23	LCD_GND	LCD logic and driver ground
24	LCD_GND	LCD logic and driver ground
25	LCD_GND	LCD logic and driver ground
26	LCD_GND	LCD logic and driver ground
27	HPD	HPD signal pin
28	BL_GND	Backlight ground
29	BL_GND	Backlight ground
30	BL_GND	Backlight ground
31	BL_GND	Backlight ground
32	BL_ENABLE	Backlight On/Off
33	BL_PWM_DIM	System PWM
34	NC	Reserved for LCD manufacturer's use
35	NC	Reserved for LCD manufacturer's use
36	VBL	Backlight power
37	VBL	Backlight power
38	VBL	Backlight power
39	VBL	Backlight power
40	OD_EN	OD Enable Signal of YCON

KBC/EC/uP (ENE9028)

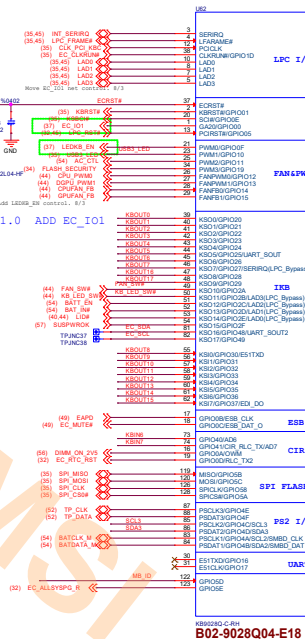
Hardware Reset

PU/PD

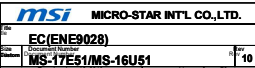
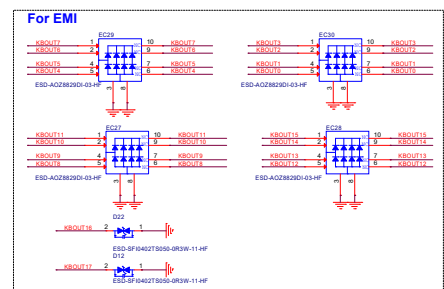
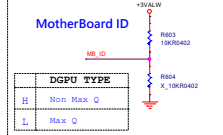
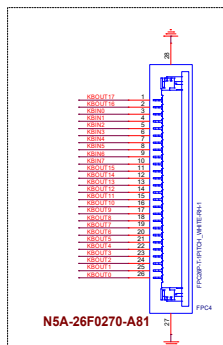
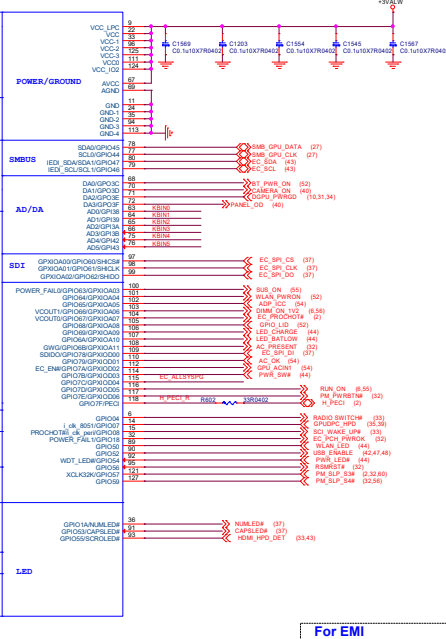


N71-0101630-D02

03/21 1.0 ADD EC_I01



B02-9028Q04-E18



ADD 022 For DMC 12/18

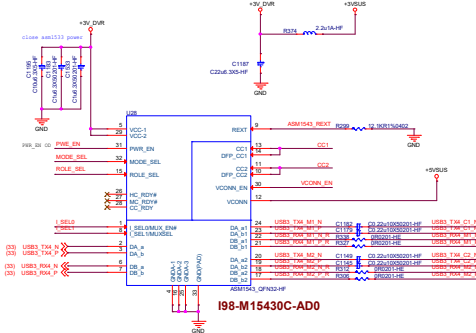
ASM1543 Mux with CCL

Function Table

Function	Signal	Level
Power	VBUS	5V
Ground	GND	0V

Strapping Table

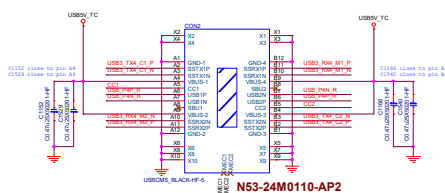
Strapping	Signal	Level
Power	VBUS	5V
Ground	GND	0V



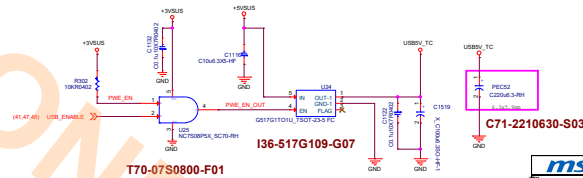
USB20 CMC



Type-C Connector

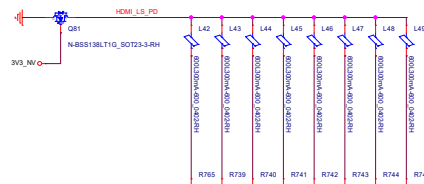


PWR Switch



ESD

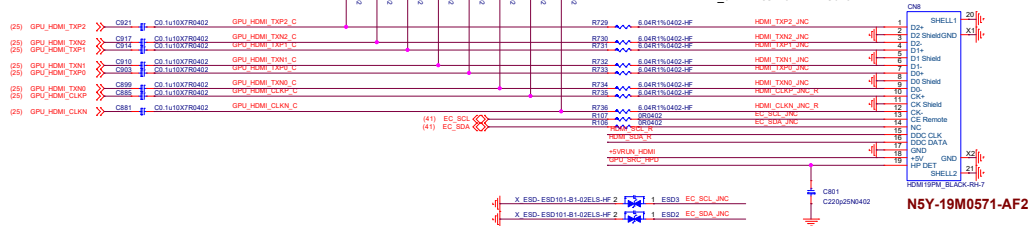




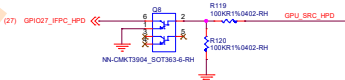
HDMI connector

An HDMI Source shall have +5V Power signal over-current protection of no more than 0.5A.

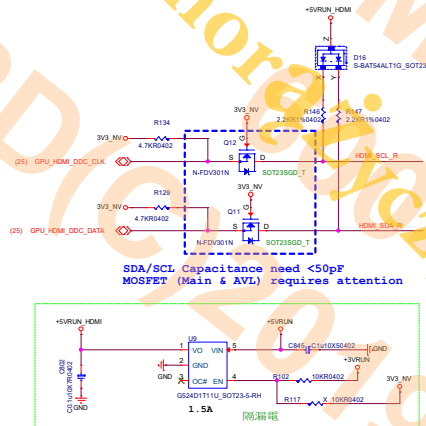
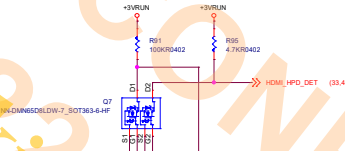
HPD_SNK Internal PD 150kohm



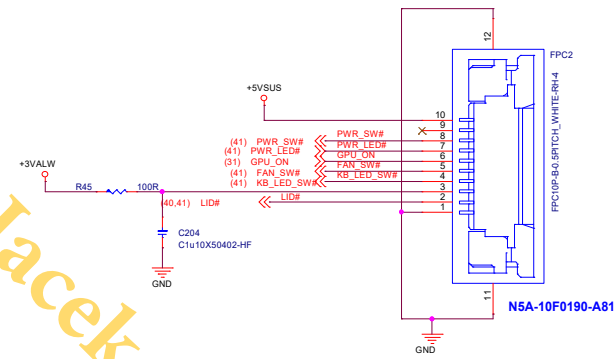
HPD Level Shift to 1.8V FOR GPU



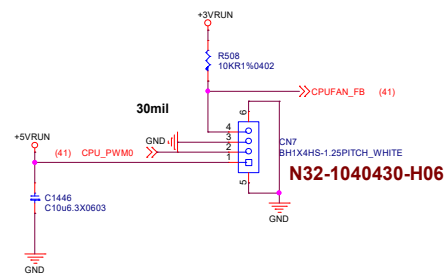
HPD Level Shift to 3V FOR PCH & EC



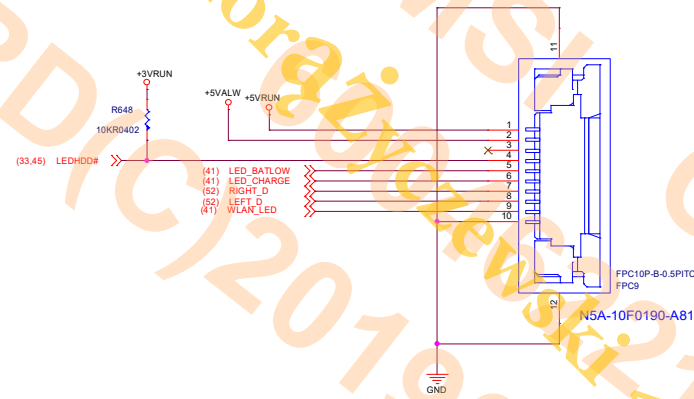
Power Switch Connector



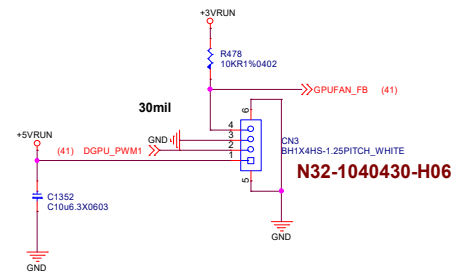
CPU FAN



Switch connector



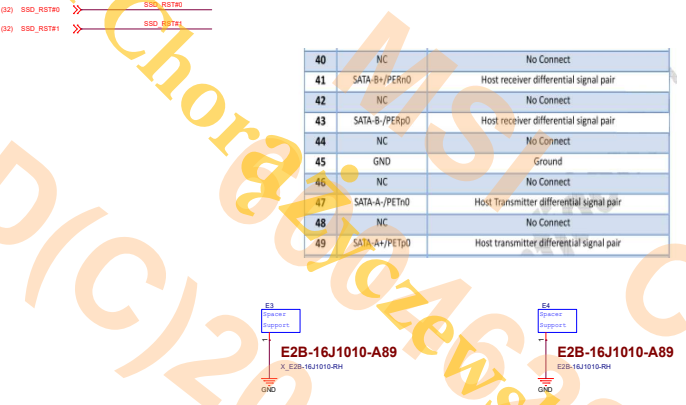
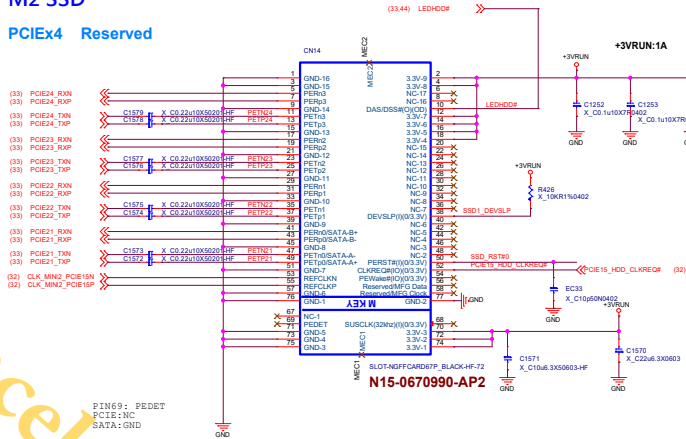
DGPU FAN



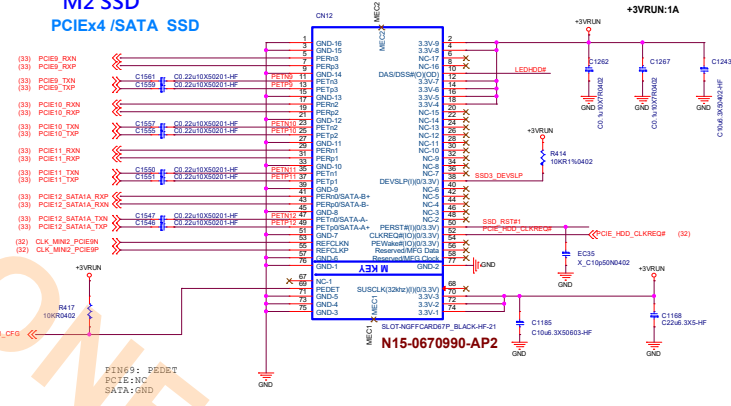
msi MICRO-STAR INT'L CO.,LTD.			
File:	CPU FAN/BTB CONN/LED		
Docu-ment Number:	MS-17E51/MS-16U51		
Date:	Tuesday, June 18, 2016	Page:	44 of 79

M2 SSD

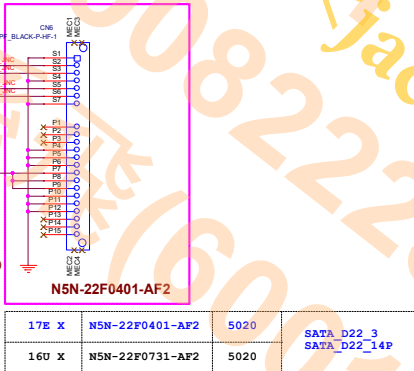
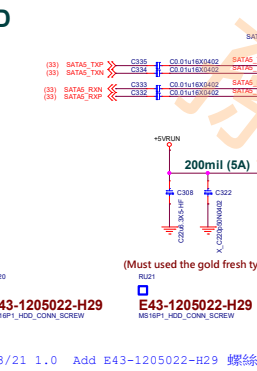
PCIEx4 Reserved



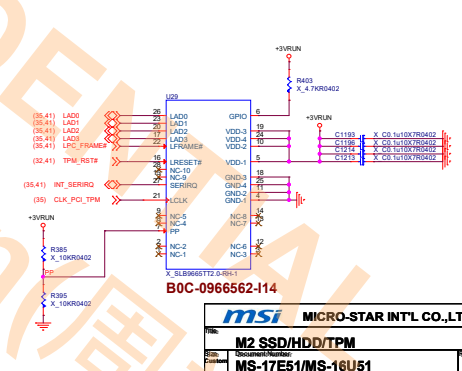
M2 SSD PCIEx4 / SATA SSD



HDD

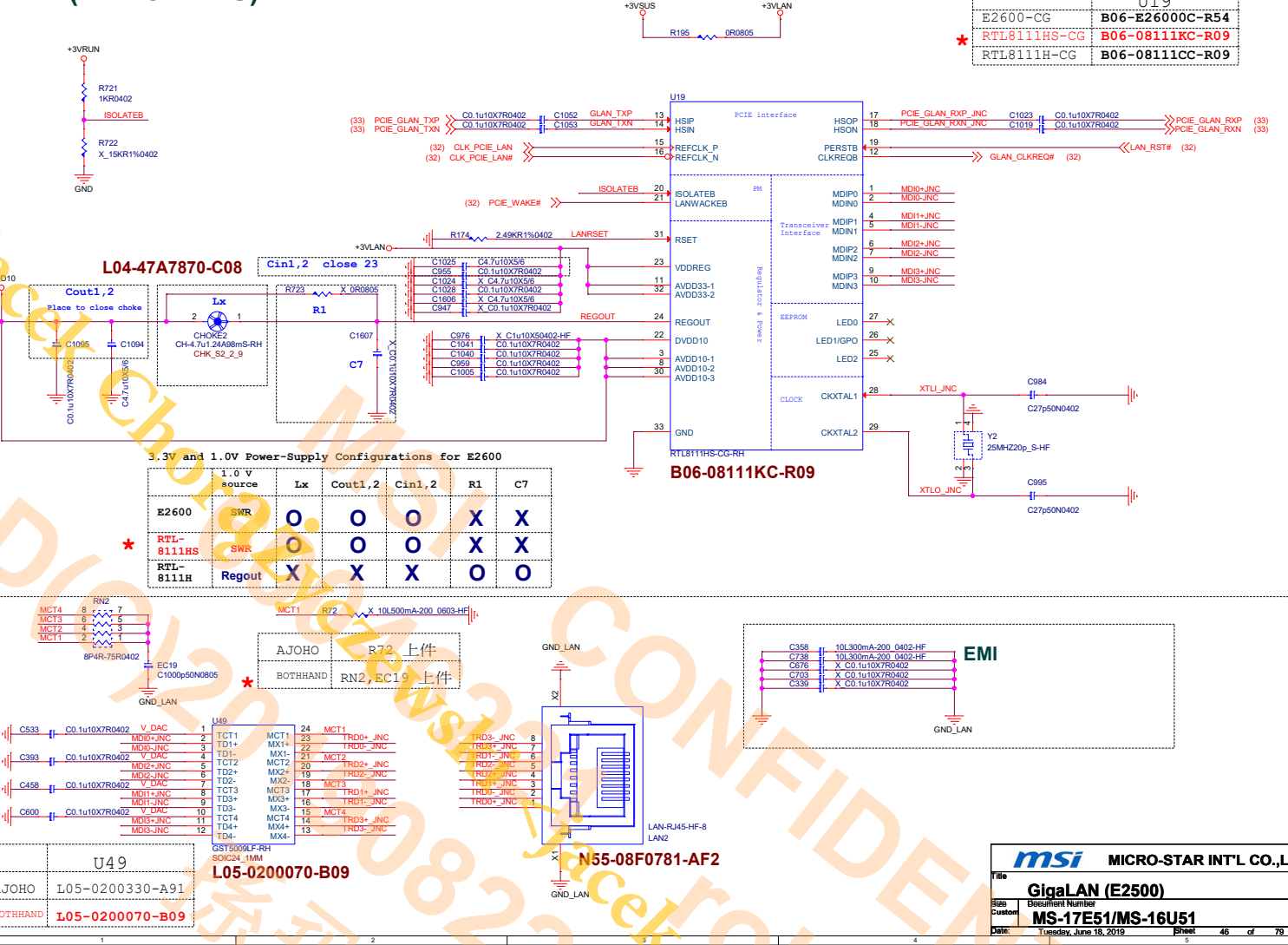


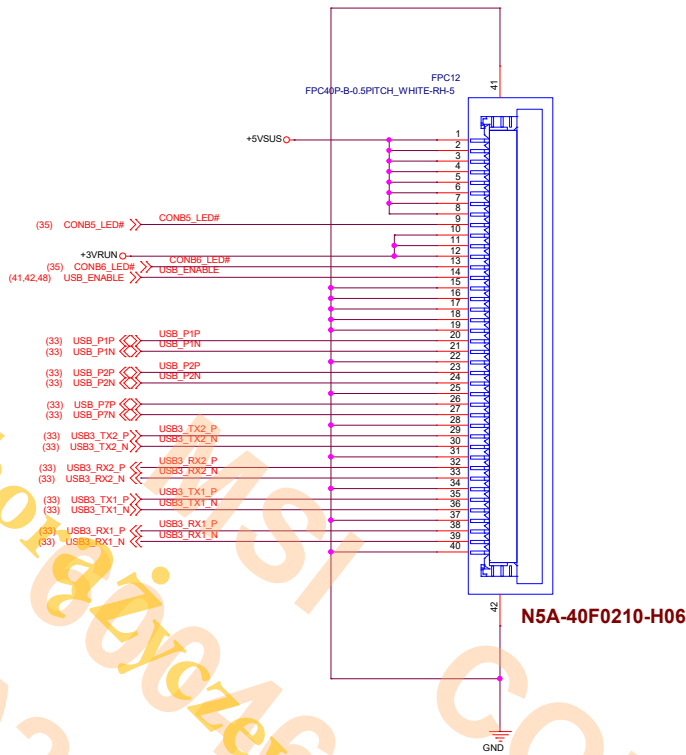
TPM



03/21 1.0 Add E43-1205022-H29 螺絲

LAN (RTL-8111HS)



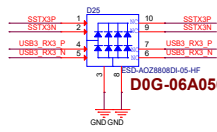


msi MICRO-STAR INT'L CO.,LTD.	
File B to B connector	
Size	Document Number
Customer	MS-17E51/MS-16U51
Date	Tuesday, June 18, 2019
Sheet	47 of 79
Rev	10

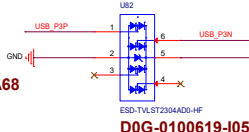
USB 3.1 CNT 3

(33) USB3_TX3_P C1090 C0.1u10X7R0402 SSTX3P
(33) USB3_TX3_N C1090 C0.1u10X7R0402 SSTX3N
(33) USB3_RX3_P USB3_RX3_P
(33) USB3_RX3_N USB3_RX3_N

USB3_RX3_P R223 X_200KR201-HE
USB3_RX3_N R228 X_200KR201-HE



D0G-06A050C-A68



D0G-0100619-I05

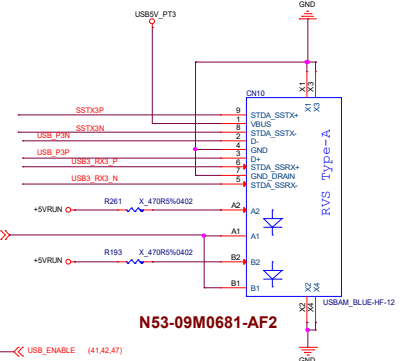
USB3V_PT3

USB3V_PT3

C71-101064G-S03

20190605 Change for inrush current

I36-5478102-G07
G547811 MAX : 2.5A



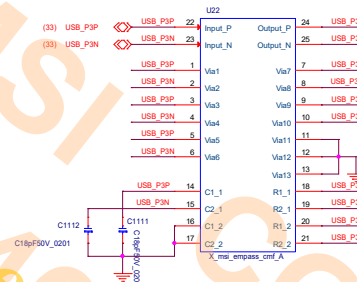
N53-09M0681-AF2

USB3_0_LED	60	N53-13M0031-L06	USB_A1_13_USB3_DP
USB3_0	50X0	N53-09M0681-AF2	Co-layout use
USB3_1_GEN2	50X0	N53-09M1021-AF2	USB_A1_9_USB3_0_1P
USB3_1_GEN2_LED	60	N53-13M0041-L06	USB_A1_11_USB3_0_1P

GE	N53-13M0041-L06
GP/GL/WE	N53-09M1021-AF2



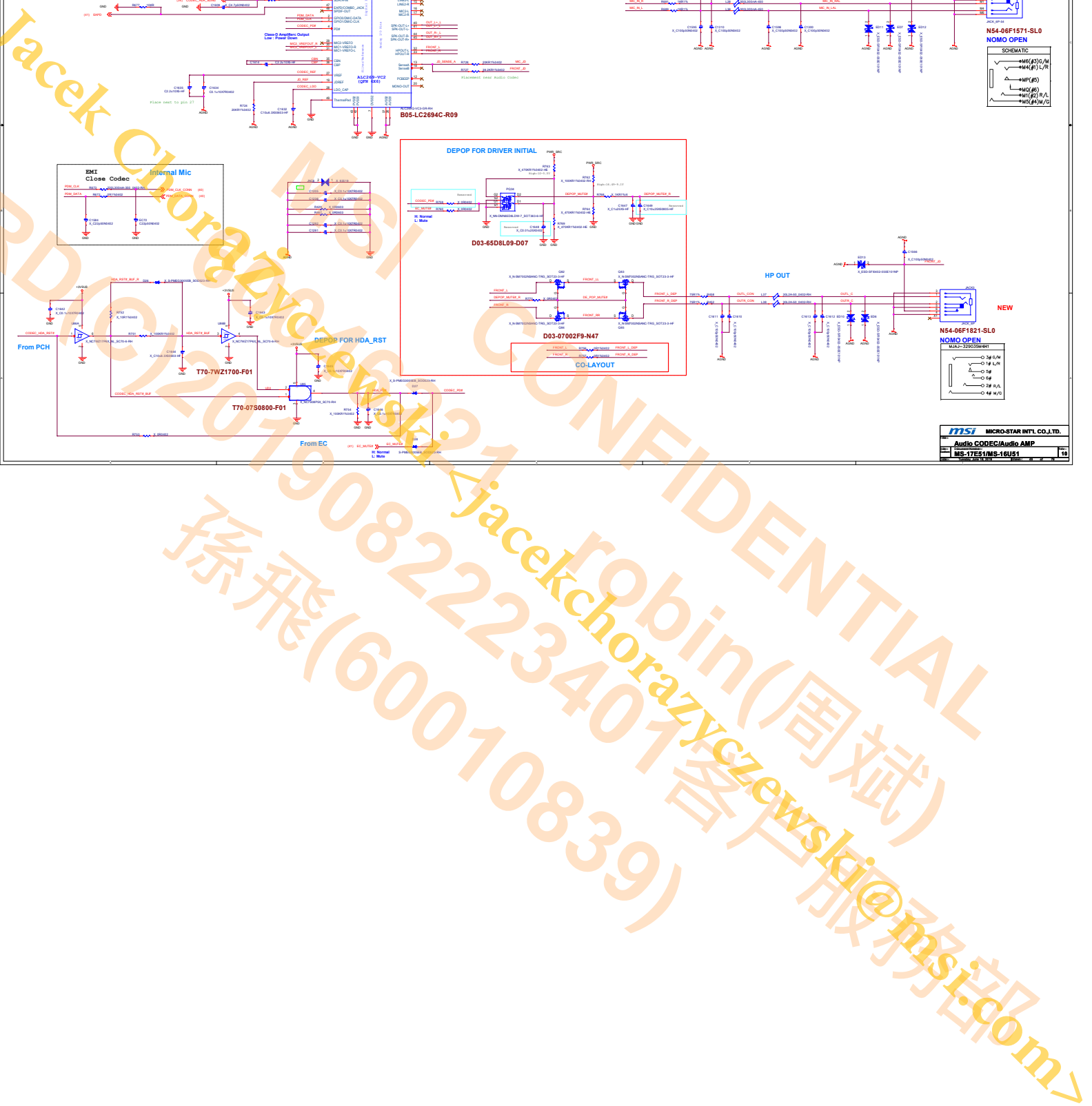
CMF ROYALTY SURPASS
Y01-REMPAS1-000

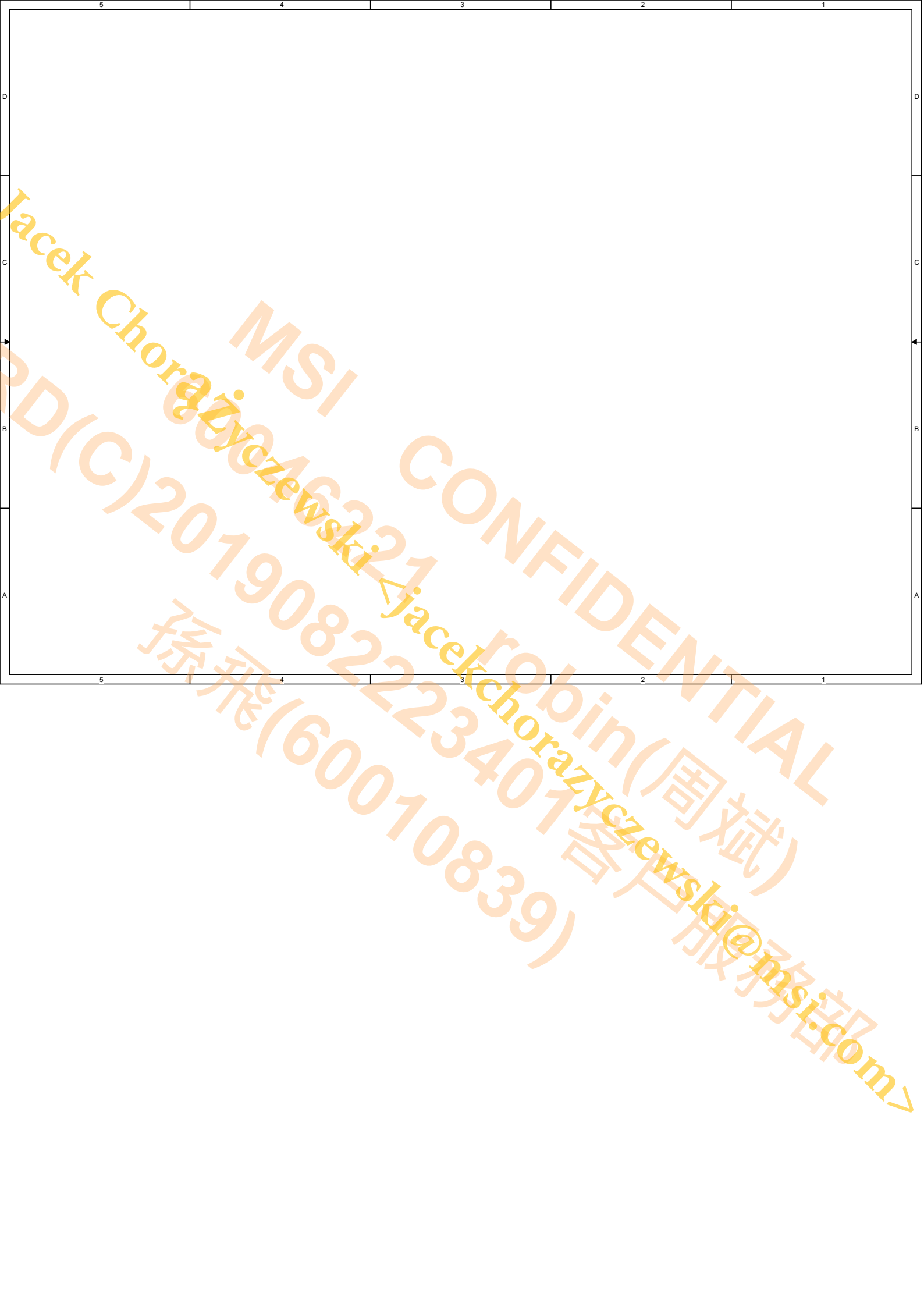


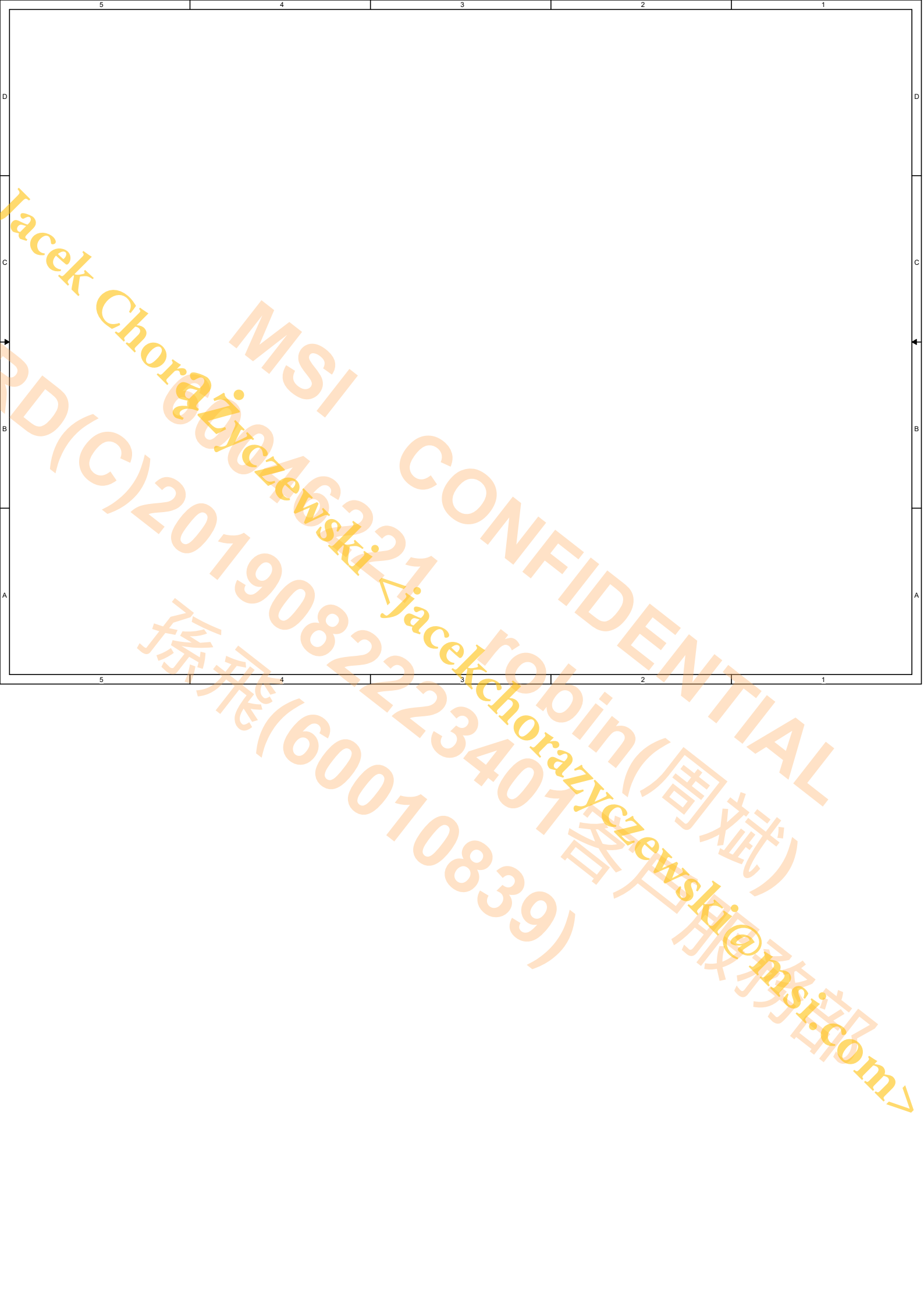
C1112

msi MICRO-STAR INT'L CO.,LTD.	
USB 3.1 connector	
Doc Number	MS-17E51/MS-16U51
Date	January, June 15, 2019

10



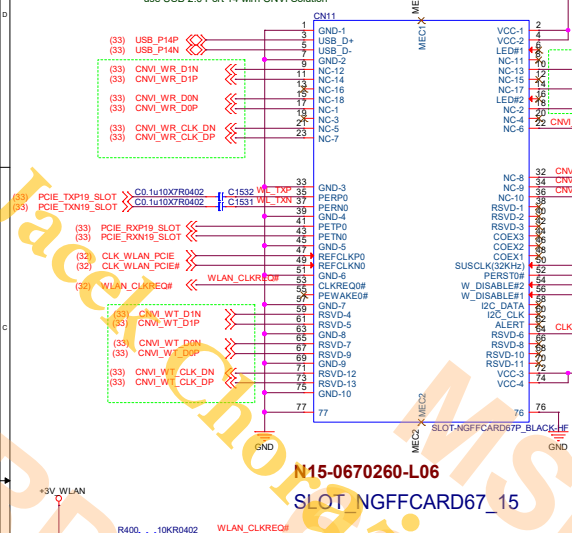




WLAN /Touch Pad

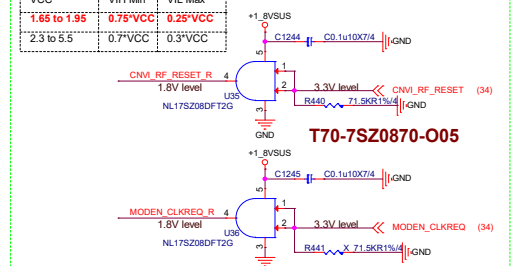
WLAN

Ref DG Section 18.6
- use USB 2.0 Port 14 with CNVI Solution

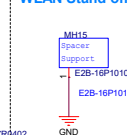


PN : T70-TS20870-005
AND Gate/ NL17S208DF2G

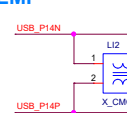
VCC	VIH Min	VIL Max
1.65 to 1.95	0.75VCC	0.25VCC
2.3 to 5.5	0.7VCC	0.3VCC



WLAN Stand off



EMI

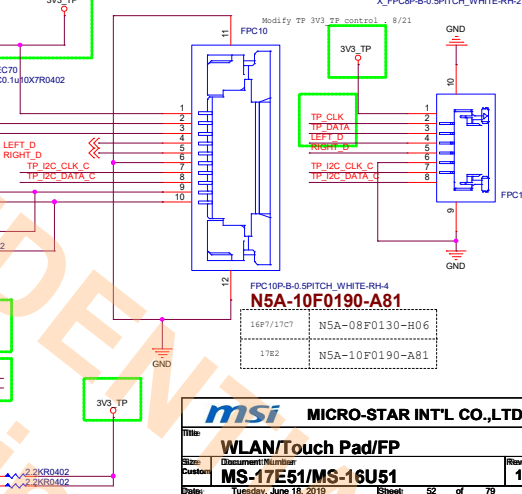
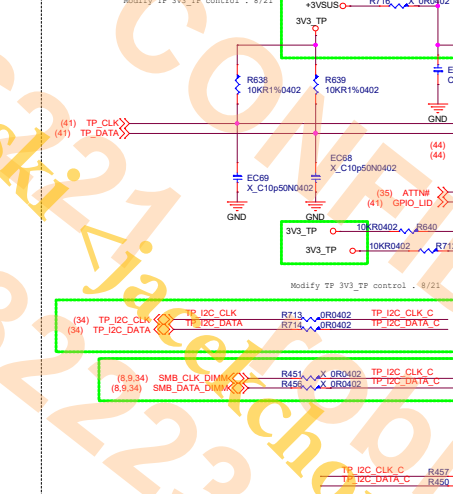
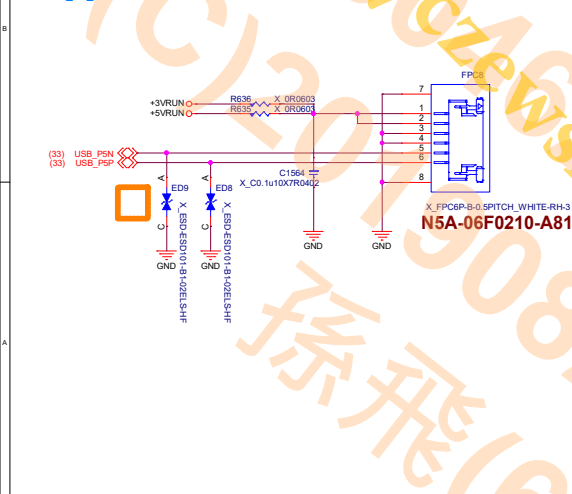


FP

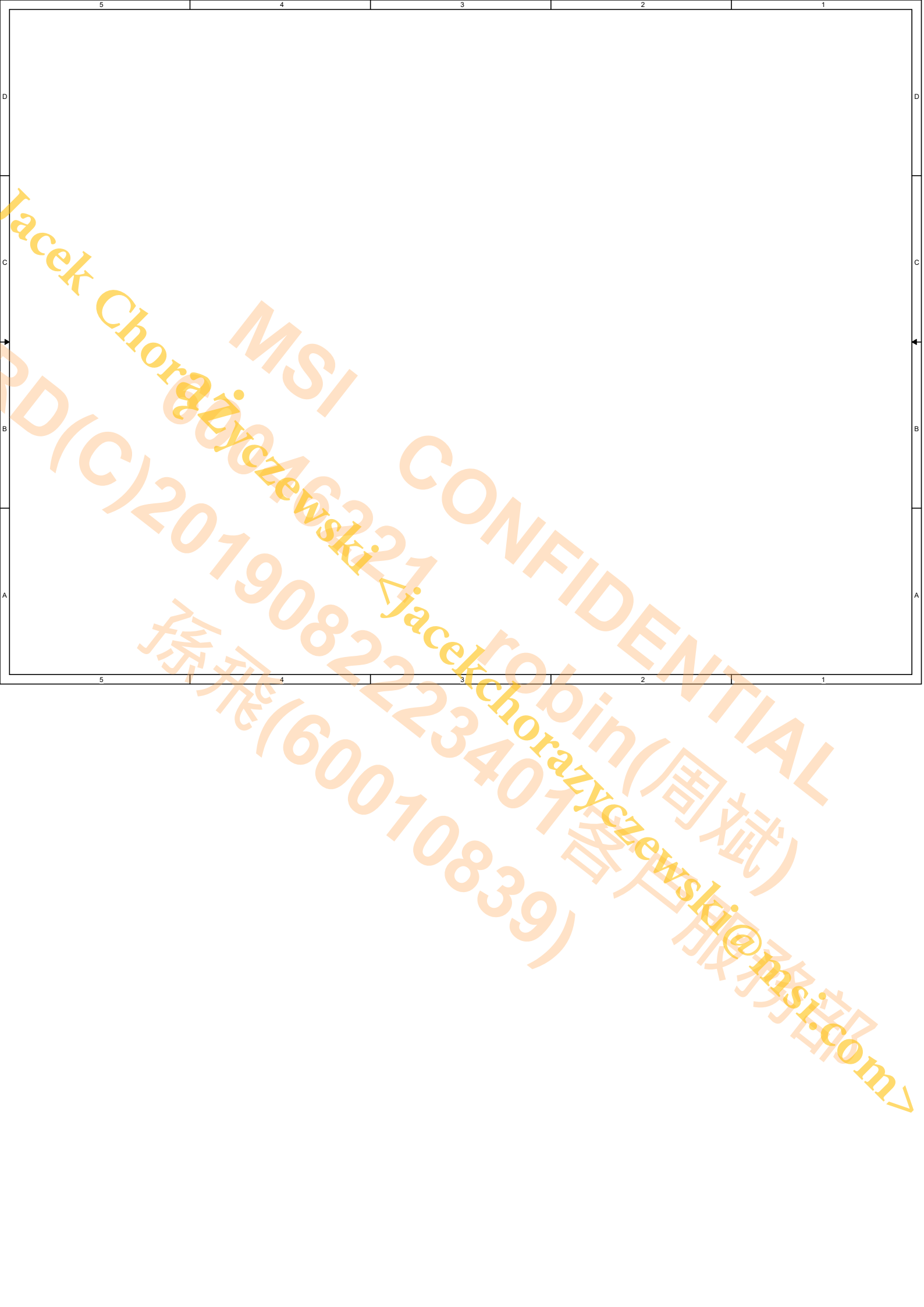
Touch Pad

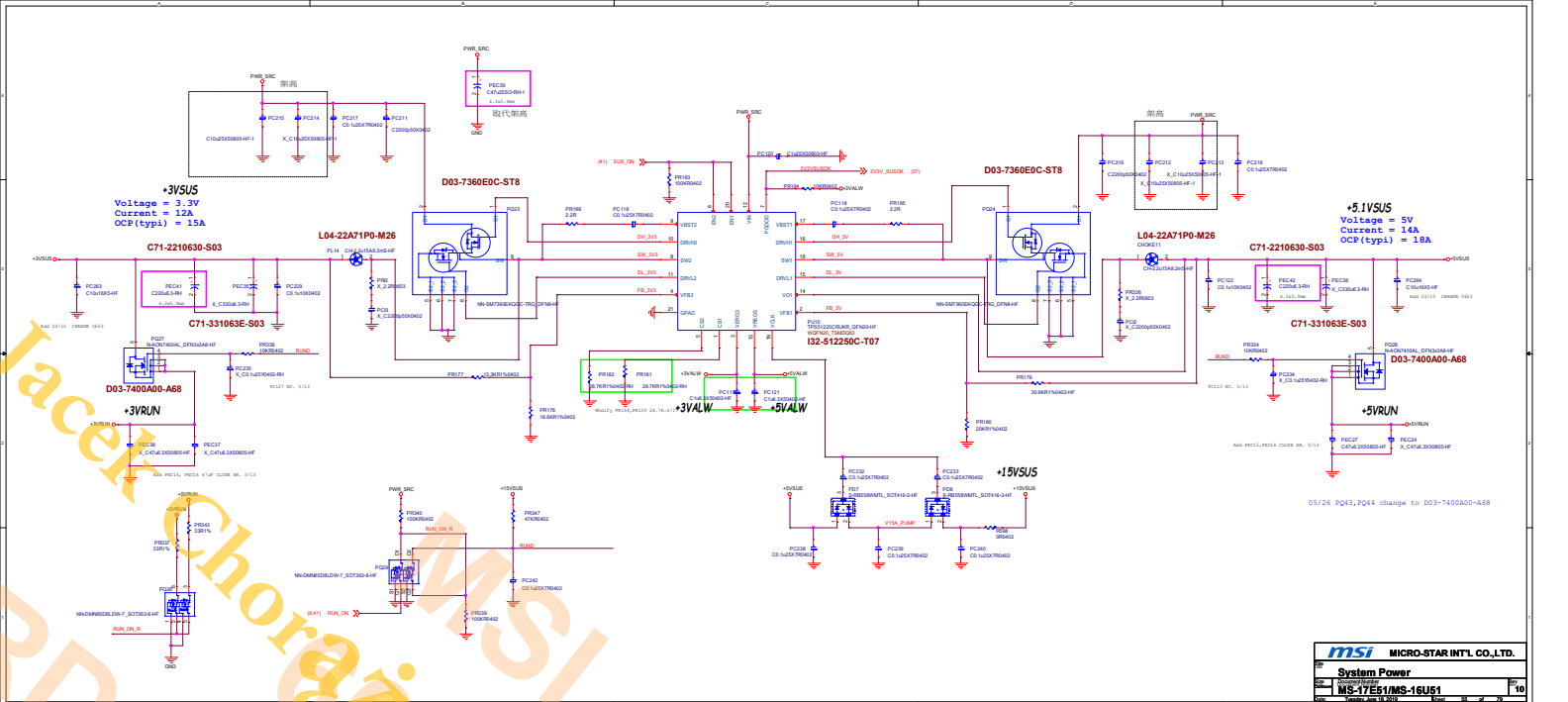
FOR 17E2

N5A-08F0130-H06



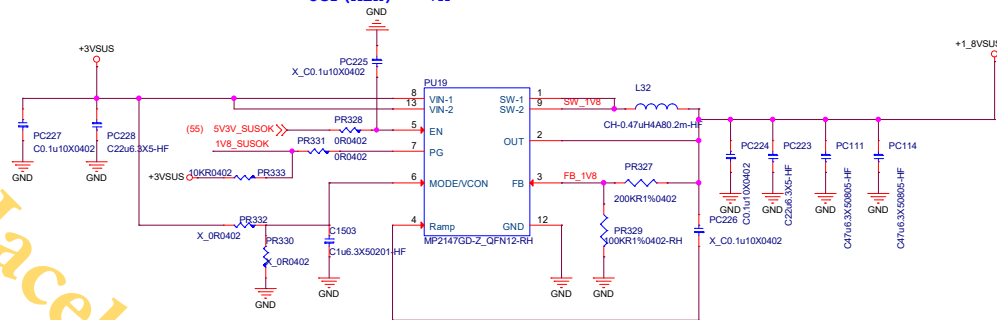
msi MICRO-STAR INT'L CO.,LTD.	
Title: WLAN/Touch Pad/FP	
Size: MS-17E51/MS-16U51	Rev: 10
Date: Tuesday, June 18, 2019 Sheet: 52 of 70	





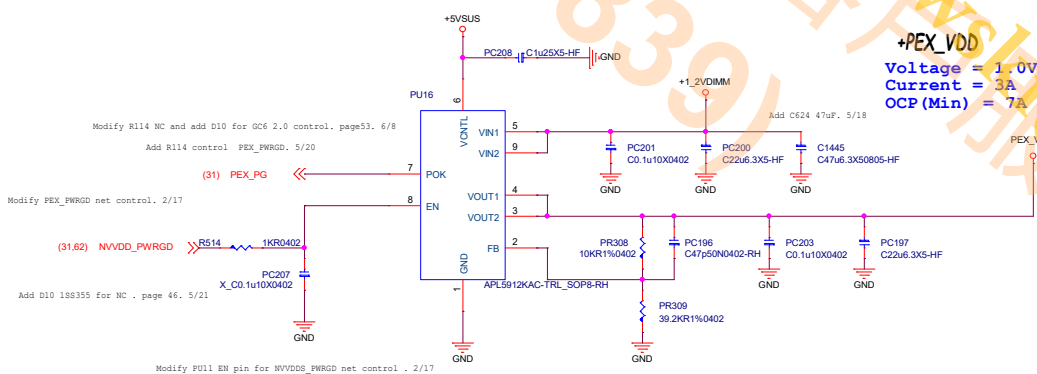
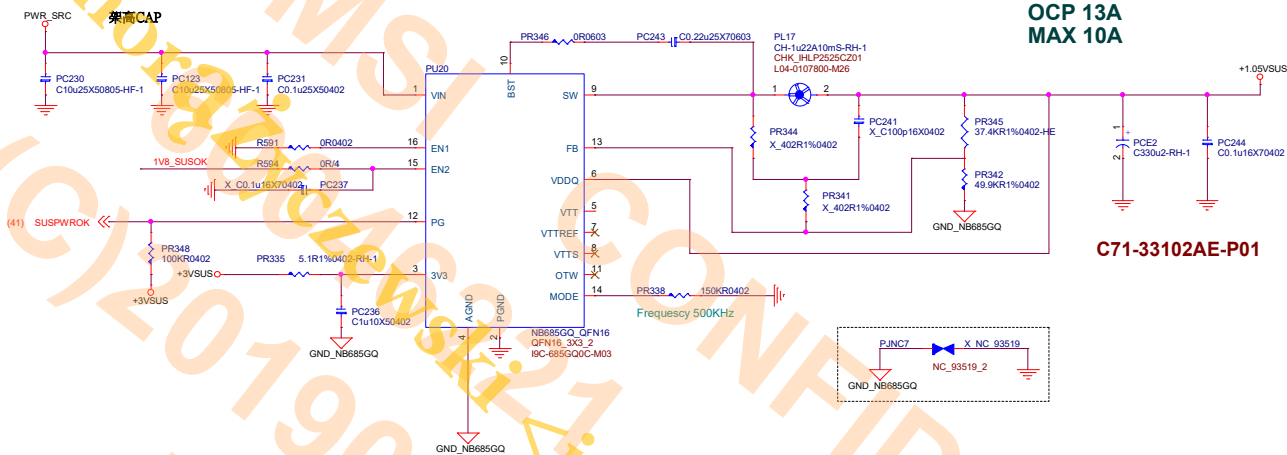
+1_8VSUS

Voltage = 1.8V
Current = 4A
OCP (Min) = 7A



+1.05VSUS

OCP 13A
MAX 10A



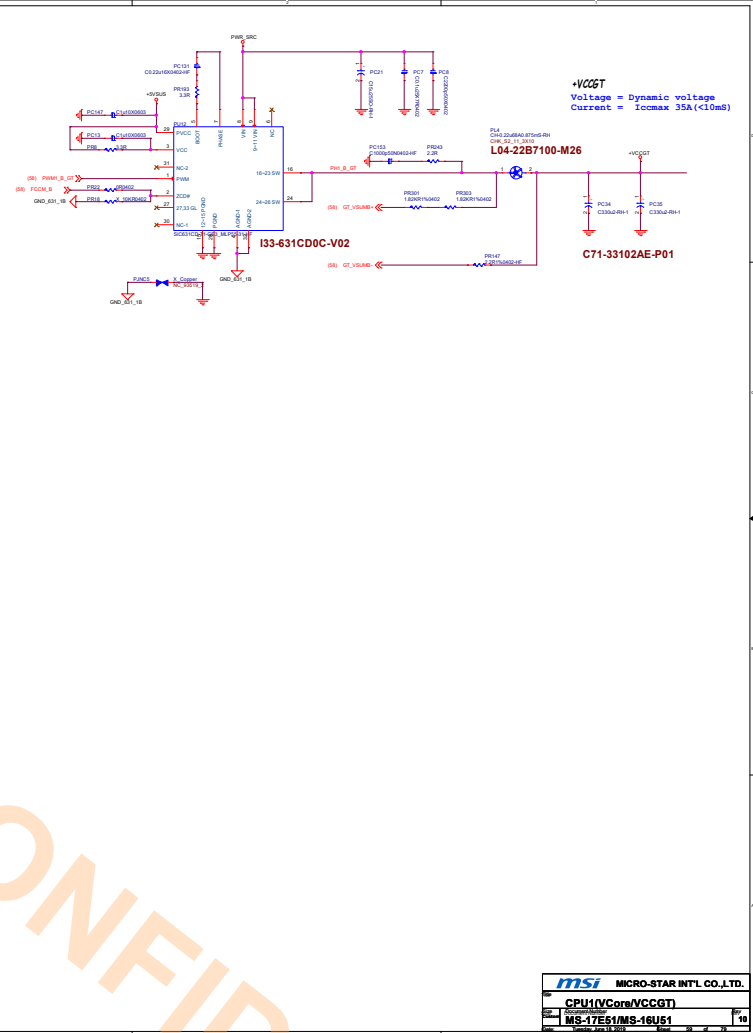
Coffee Lake H-line
62 45W ISL95855C



```

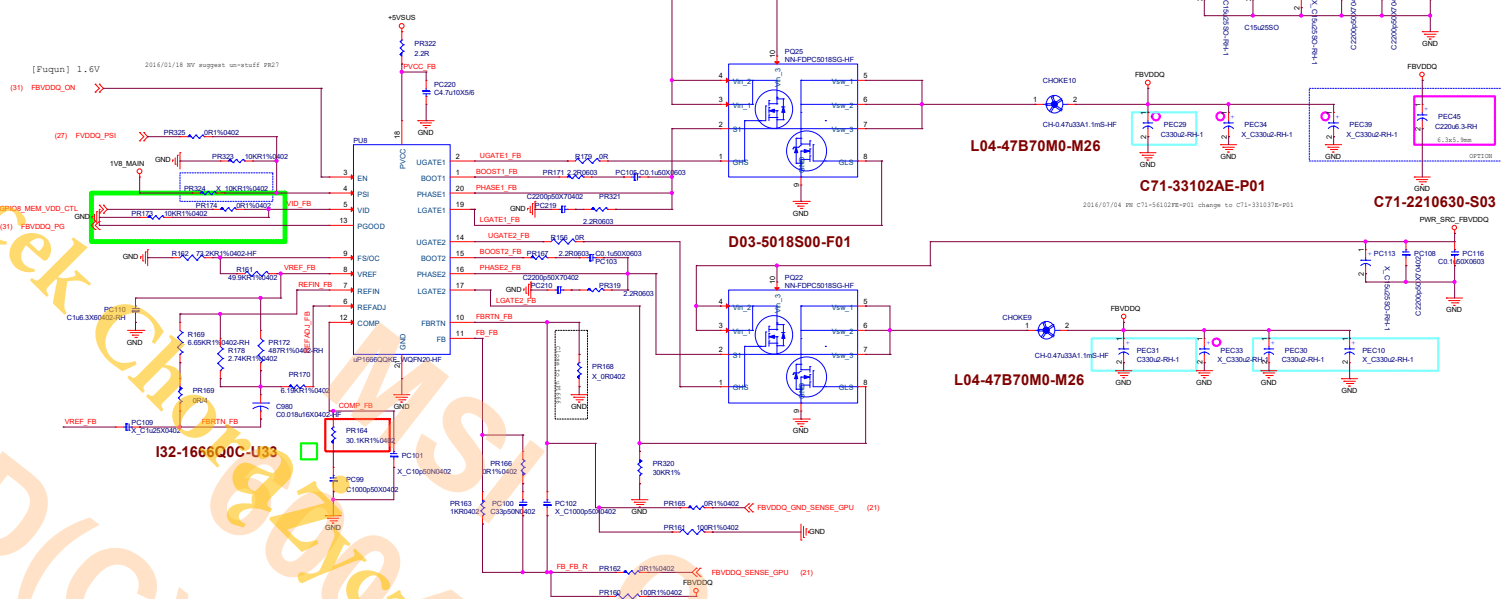
PROG1 310KR  Vboot=0V, Selv_rate=30mV/us, VR_A=1A, VR_B=UT, VR_C=SA
PROG2 78.7KR  IMAX VR_A=1A, VR_B=1A FSI=1PH
PROG3 34KR    IMAX VR_B=1A, DROOF VR_B Active
PROG4 182KR   DROOF VR_A Active, DROOF VR_C Active, VR_A VR_B Frequency=750KHz
PROG5 34KR    IMAX VR_C=1A, frequency=50KHz


```



EDP-Con 28A

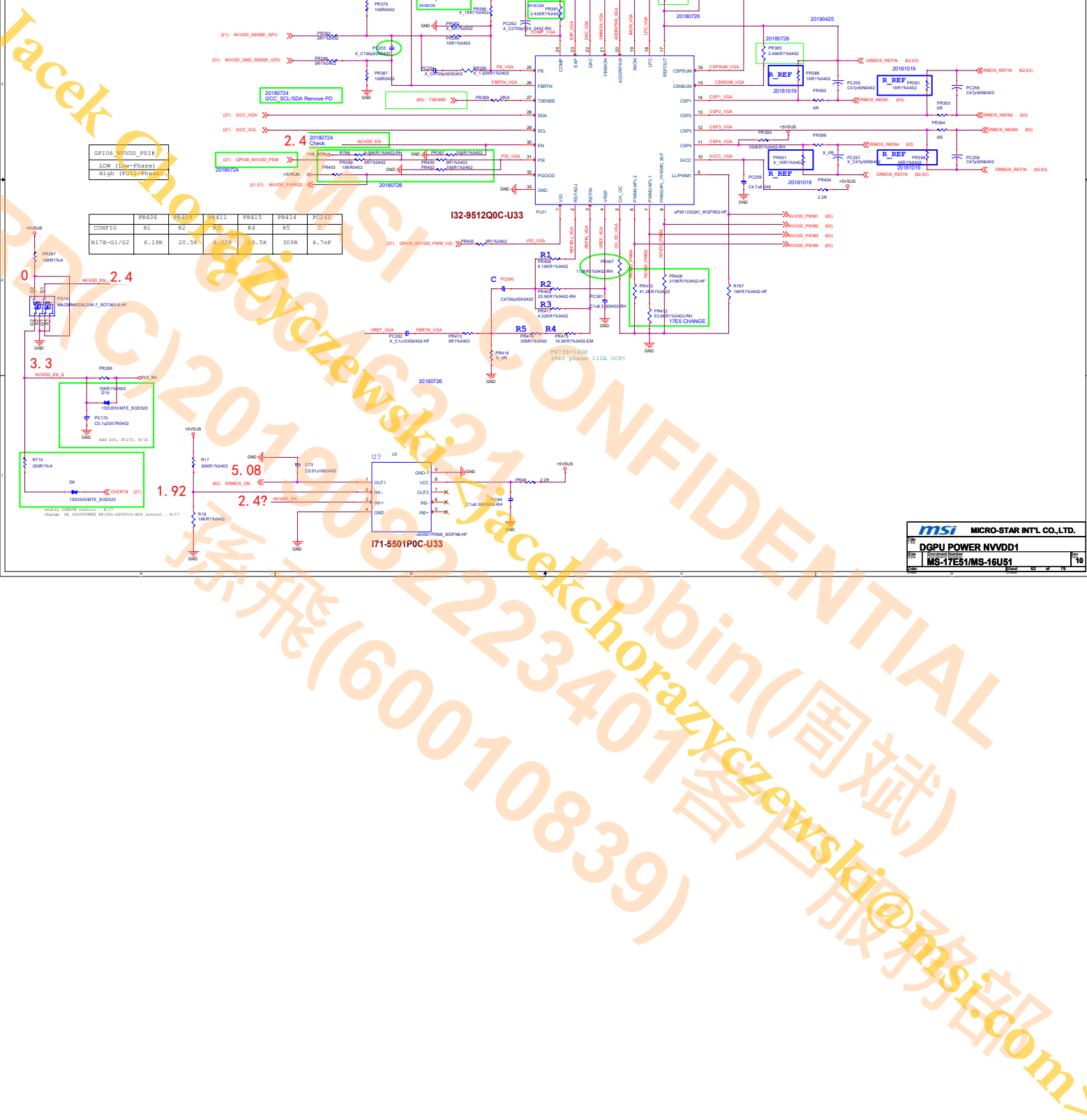
VBoot:1.35V
Vmin:1.25V / Vmax:1.35V



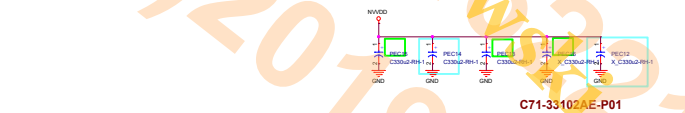
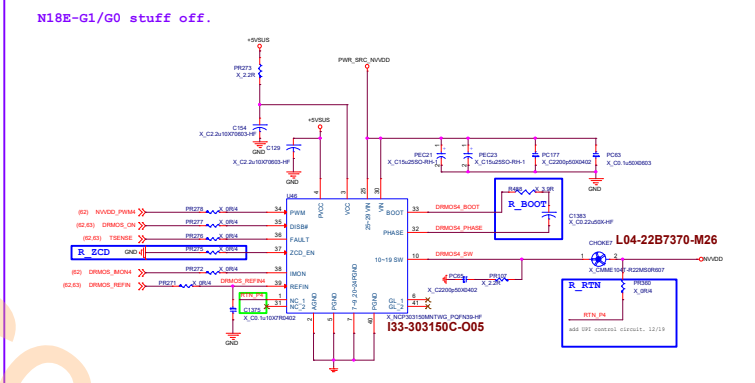
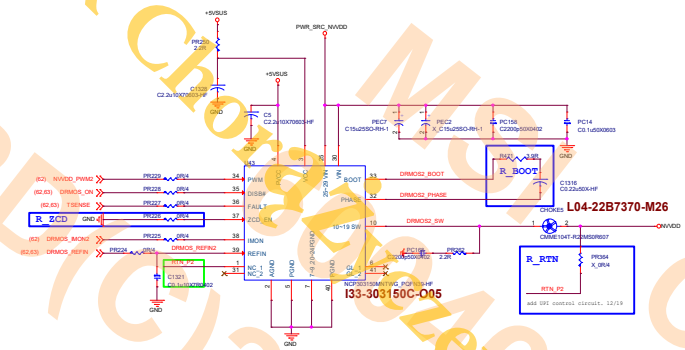
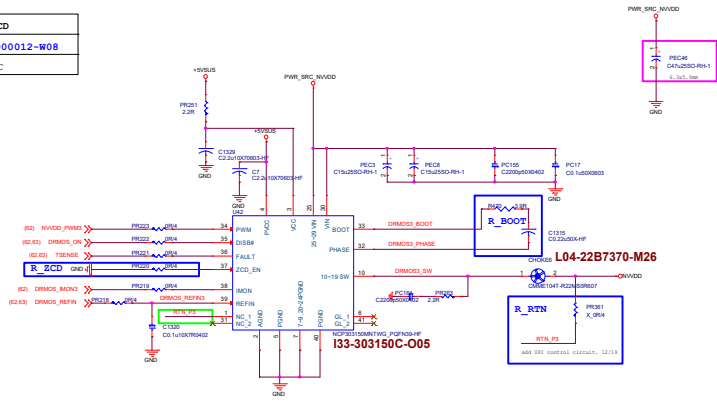
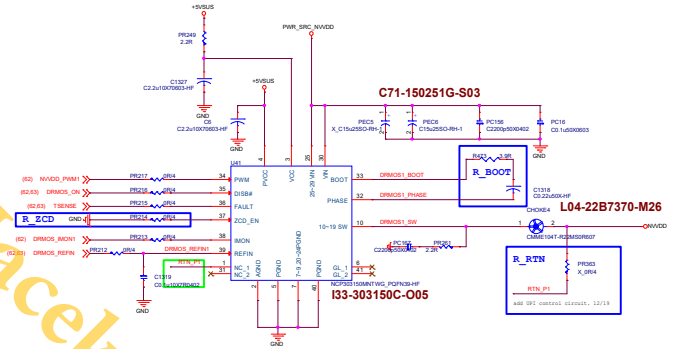
 MICRO-STAR INT'L CO., LTD.	
DGPU POWER FBVDDQ1	
Document Number MS-17E51/MS-16U51	Rev 10

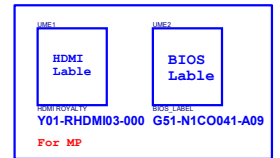
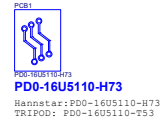
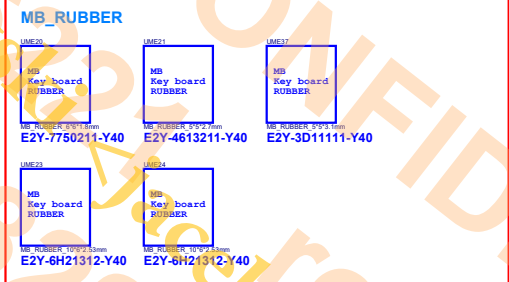
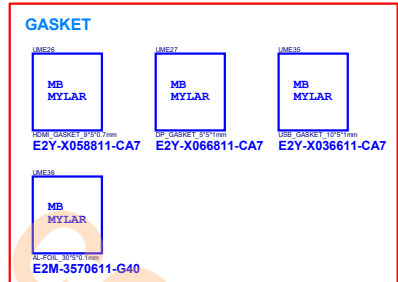
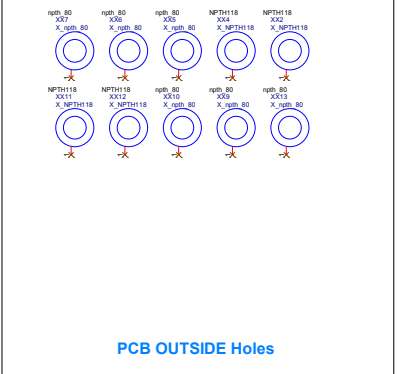
VBOOT:0.8V
Vmin:0.3V / Vmax:1.3V

Dr.mos PN	R_REF
ON Semi	1K R11-0102T12-W08
UPI	NC



	Dr.mos PN	R_BOOT	R_RTN	R_ZCD
ON Semi	I33-303150C-005	3.9R R11-039A033-W08	NC	OR R11-0000012-W08
UPI	I33-9619A0C-047	2.2R R11-022A013-W08	OR R11-0000012-W08	NC

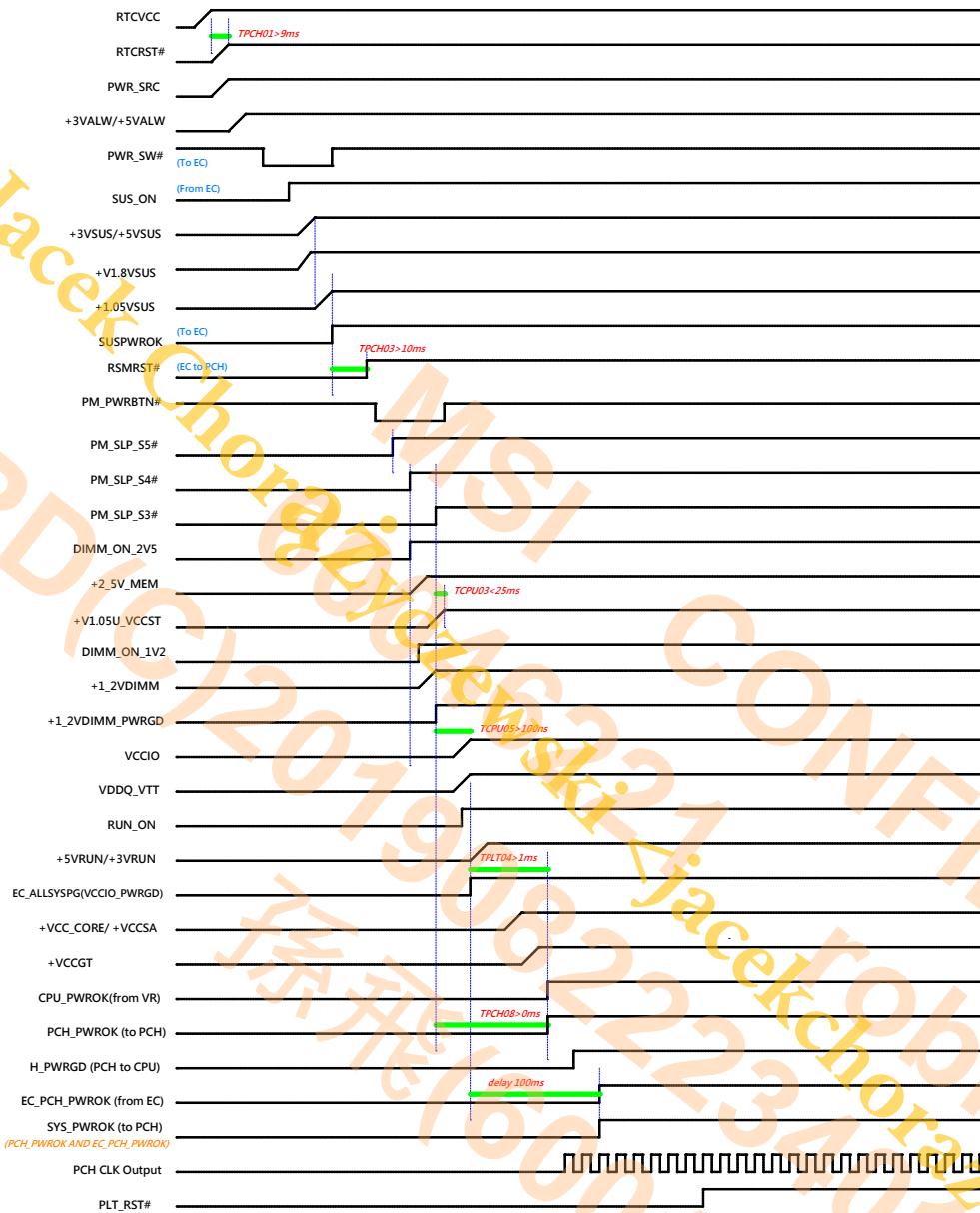




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PD(C)2019082223401
孫飛(60010839)
robins(周文斌)
客戶服務部

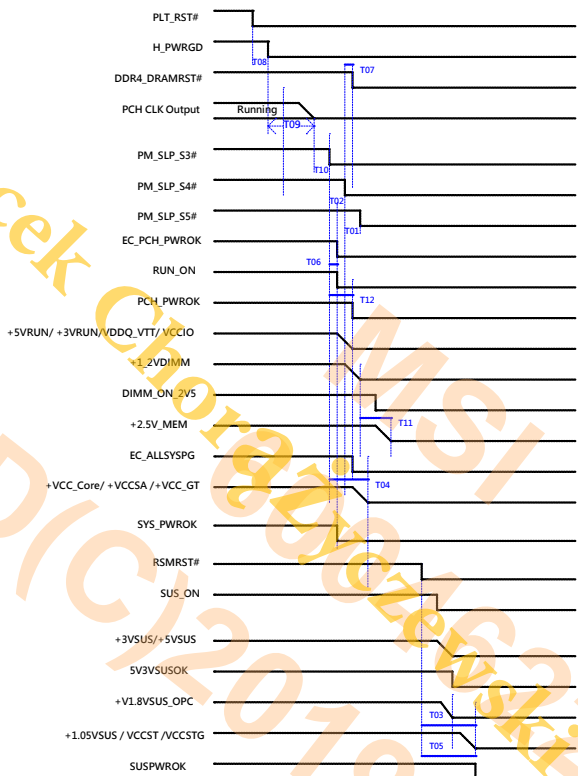
Power on Sequence

G3 -> S0



Power down Sequence

S0 -> G3



	MIN	MAX	Units	Description
T01	30		us	SLP_S5# assertion to SLP_S4#
T02	30		us	SLP_S4# assertion to SLP_S3#
T03	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T04		500	ms	SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.
T05	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T06		1	us	SLP_S3# assertion to VCCIO VR disabled
T07	-100		ns	DDR_RESET# assertion to SLP_S4# assertion
T08	30		us	PLTRST# assertion to PROCPWRGD deassertion
T09	10		us	PROCPWRGD de-assertion to CLKOUT_BCLK turning OFF.
T10	1		us	CLKOUT_BCLK turning OFF to SLP_S3# assertion
T11	30		ms	VDDQ ramped down to VPP ramp down
T12	0		ms	SLP_S3# assertion to PCH_PWROK deassertion

The diagram illustrates the power management architecture for the MS-17E61/MS-16U51 system. It shows the interconnections between the Embedded Controller (EC, ENE9028), the Platform Controller Hub (PCH-H), the Central Processing Unit (CPU), and various power management components.

EC (ENE9028) Connections:

- Inputs:** +3VSUS (5), +2.5V_MEM (14), +5VSUS (16), +1_2VDIMM (17), +0_6VRUN (18), +5VRUN (21), +3VRUN (21), EC_ALLSYSPG (23), CPU_PWROK (25), PCH_PWROK (26), EC_PCH_PWROK (27).
- Outputs:** 5V3VSUSOK (6), DIMM_ON_2V5 (13), DIMM_ON_1V2 (15), RUN_ON (19), EC_PCH_PWROK (27), EC_ALLSYSPG (23) (VCCIO_PWRGD).
- Internal Components:** NB671LGQ-Z (DIMM control), APW8819QAI (Voltage Supervisor), SM3316 (Voltage Detector), Level Shifter, AND Gate (for PCH_PWROK and SYS_PWROK), Delay 100ms.

PCH-H Connections:

- Inputs:** RSMRST# (9), PM_PWRBTN# (10), PM_SLP_S5# (11), PM_SLP_S4# (12), PM_SLP_S3# (18), PCH_PWROK (24), SYS_PWROK (29).
- Outputs:** H_PWRGD (28), PLT_RST# (30), VCCIO_EN (22), VCCIO_PWRGD (23) (EC_ALLSYSPG).

CPU Connections:

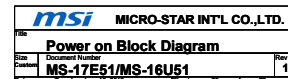
- Inputs:** +VCCGT, +VCC_CORE, +VCCSA, +VCCIO_PWRGD (23) (EC_ALLSYSPG).
- Outputs:** +VCC_CORE & +VCCSA & +VCCGT (24), CPU_PWROK (25).

ISL95855 Connections:

- Inputs:** +5VSUS, PWR_SRC, VR_ON (23) (EC_ALLSYSPG).
- Outputs:** +VCC_CORE & +VCCSA & +VCCGT (24), CPU_PWROK (25).

MSI Logo and Document Information:

File: **Power on Block Diagram**
 Size: **MS-17E61/MS-16U51**
 Date: **2012.12.18**
 Rev: **10**



MS-17E5 Revision History List

2019/03/26	VER 0A	MS-17E5_0A_2060_SAMSUNG_1903026B_1010_16.DSN (Copy From MS-16U11)	Gerber out
2019/03/26	VER 0A	MS-17E5_0A_2060_SAMSUNG_1903025D_ALL_1010_16	pre BOM
2019/03/29	VER 0A	MS-17E5_0A_2060_SAMSUNG_1903029A_1010_16.DSN	NEW BOM
2019/04/01	VER 0A	MS-17E5_0A_2060_SAMSUNG_190401A_1010_16.DSN Page 49 (BOM) :Modify L39 L38 from L02-3008012-M26 to L02-3008012-T19	
2019/04/08	VER 0A	MS-17E5_0A_2060_SAMSUNG_190408A_1010_16.DSN Page 01 (TXT) :ADD BOM TABLE Page XX (BOM) :ADD NEW BOM A02 A03 FOR PM	
2019/04/15	VER 0A	MS-17E5_0A_2060_SAMSUNG_190415A_1010_16.DSN Page 11,36 (LAYOUT) :CHANGE C1133 C1288 C1464 FOOTPRINT from C0603_MXM to NV_C0603_LARGE Page 35 (BOM) :CHANGE R63 from SOCKET to SPI ROM ,and remove U80 Page 35 (BOM) :CHANGE G602060, GPU1160 ASM LEVEL from 5010 to 5020	
2019/04/25	VER 0A	MS-17E5_0A_2060_SAMSUNG_190425A_1010_16.DSN Page 65 (BOM) :ADD UME19 For ME Request Page 49 (BOM) :Remove D27 For Post down Change R768 form 100R to 1KR For power off de-Pop Page 62 (LAYOUT) :CHANGE PU21 PIN17 Net NAME "REFOUT_VGA" to "DRMOS_REFIN"	
2019/05/07	VER 0A	MS-17E5_0A_2060_SAMSUNG_190507A_1010_16.DSN Page 63 (BOM) : Stuff PEC3 .PEC14 For power Request Page 61 (BOM) : Stuff PEC40 For power Request Page 62 (BOM) : Change PC246 Form 700P to 150P PR412 Form 61.9K to 53.6K PR410 Form 52.3K to 41.2K For power Request Page 65 (BOM) : Add UME20-UME24 For ME Key board Request Page 49 (BOM) : Stuff ED14-ED17 C11-6812812-W08 For EMI Request	
2019/05/10	VER 10	MS-17E5_10_2060_SAMSUNG_190510A_16 .DSN Page 55 (LAYOUT) : Change PC263 PC264 From C11-1067412-W08 to C11-1067513-W08 For Power	Change DSN to 1.0 VER
2019/05/23	VER 10	MS-17E5_10_2060_SAMSUNG_190523A_16.DSN Page 73 (BOM) : Change RB2, RB3, RB4, RB5, RB8, RB9 FROM 0R to 22R For SA Over/Undershoot Page 65 (BOM) : Stuff UME1, UME2 For MP PROJECT Page 55 (BOM) : Stuff PC215 For Power request Page 63 (BOM) : remove nvdd pahse 4 Components Page 76 (BOM) : Stuff EDC5 (D0G-03A0550-SI0) For EMI Request Page 49 (BOM) : remove ADUIO DE-POP Components	Gerber out
2019/05/30	VER 10	MS-17E5_10_2060_SAMSUNG_190530A_166.DSN Page XX (BOM) : ADD NEW CFG ,And Change 1.0 PCB PN	NEW BOM
2019/06/05	VER 10	MS-17E5_10_2060_SAMSUNG_190605A_166.DSN Page 65 (BOM) : ADD UME25 For ME Request Page 48,74 (BOM) : Change EC55, ECB10, ECB11 form C11-4767314-M09 47uF to C11-1077314-M09 100uF for USB ODD inrush current	

MS-16U5 Revision History List

2019/06/05	VER 10	MS-16U5_10_2060_SAMSUNG_190605A_166 .DSN Page XX (BOM) : Copy Main board to 16U5 forom MS-17E5_10_2060_SAMSUNG_190605A_166.DSN Page XX (BOM) : Copy A B C board to 16U5 forom MS-16U1_10_2060_SAMSUNG_i5-9300H_190521_1849_16_Final sent to layout .DSN Page XX (TXT) : Change A B C board to 16U5 forom MS-16U1_10_2060_SAMSUNG_i5-9300H_190521_1849_16_Final sent to layout .DSN	
2019/06/11	VER 10	ms-16u5_10_2060_samsung_190611A_166 Page 73 (BOM) : Change RB2, RB3, RB4, RB5, RB8, RB9 FROM 0R to 22R For SA Over/Undershoot Page 48,74 (LAYOUT) : Change EC55, ECB10, ECB11 form C11-4767314-M09 47uF to C71-101064G-S03 100uF for USB ODD inrush current	Gerber out
2019/06/12	VER 10	ms-16u5_10_2060_samsung_190612A_166 Page 73 (BOM) : Change 16U5 Excipient For ME Request	
2019/06/13	VER 10	ms-16u5_10_2060_samsung_190613A_166 Page 76 (BOM) : Stuff EDC5 (D0G-03A0550-SI0) For EMI Request	pre BOM
2019/06/18	VER 10	ms-16u5_10_2060_samsung_190618A_166 Page XX (BOM) : Change 1.0 PCB PN Page 45 (BOM) : Change CN12 CN14 PN From N15-0670320-CK3 to N15-0670990-AP2	NEW BOM
2019/06/24	VER 10	ms-16u5_10_2060_samsung_190624A_166 Page 65 (BOM) : ADD UME37 For ME Request	

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File

History

Doc

Doc Number

MS-17E51/MS-16U51

Rev

10

Date

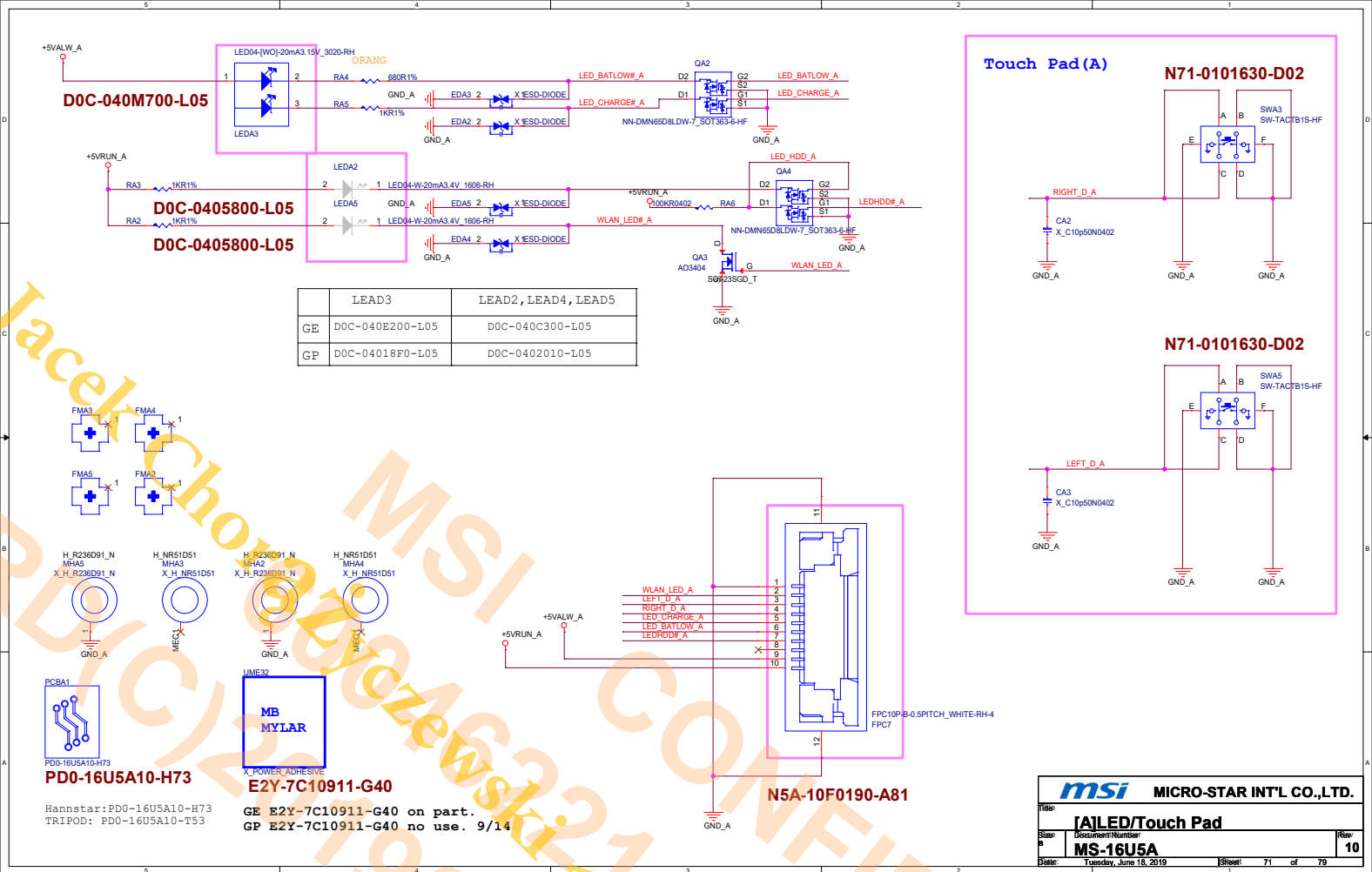
Friday, June 21, 2019

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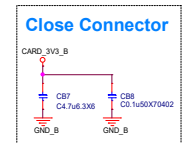
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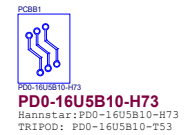
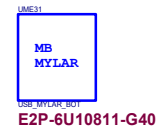
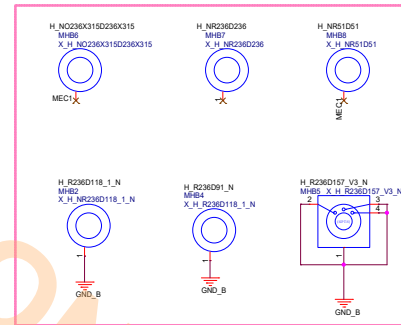
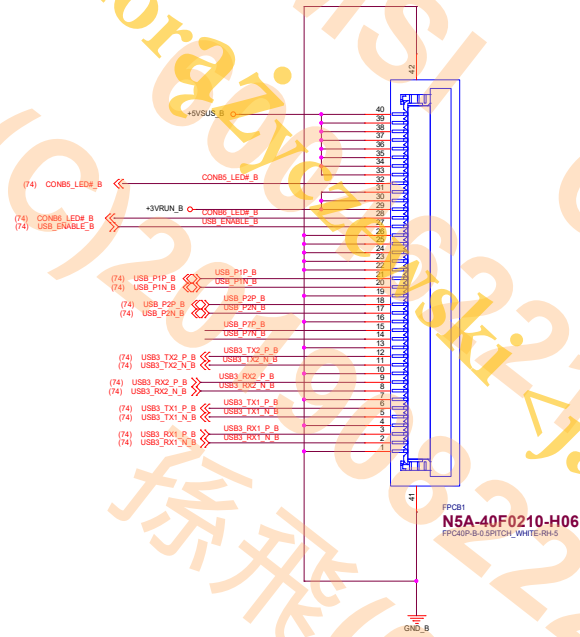



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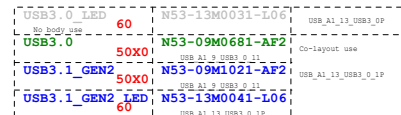
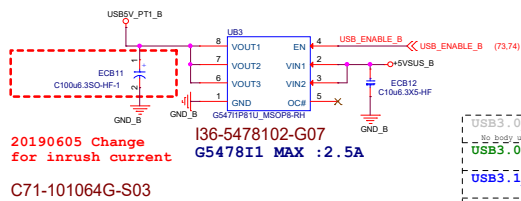



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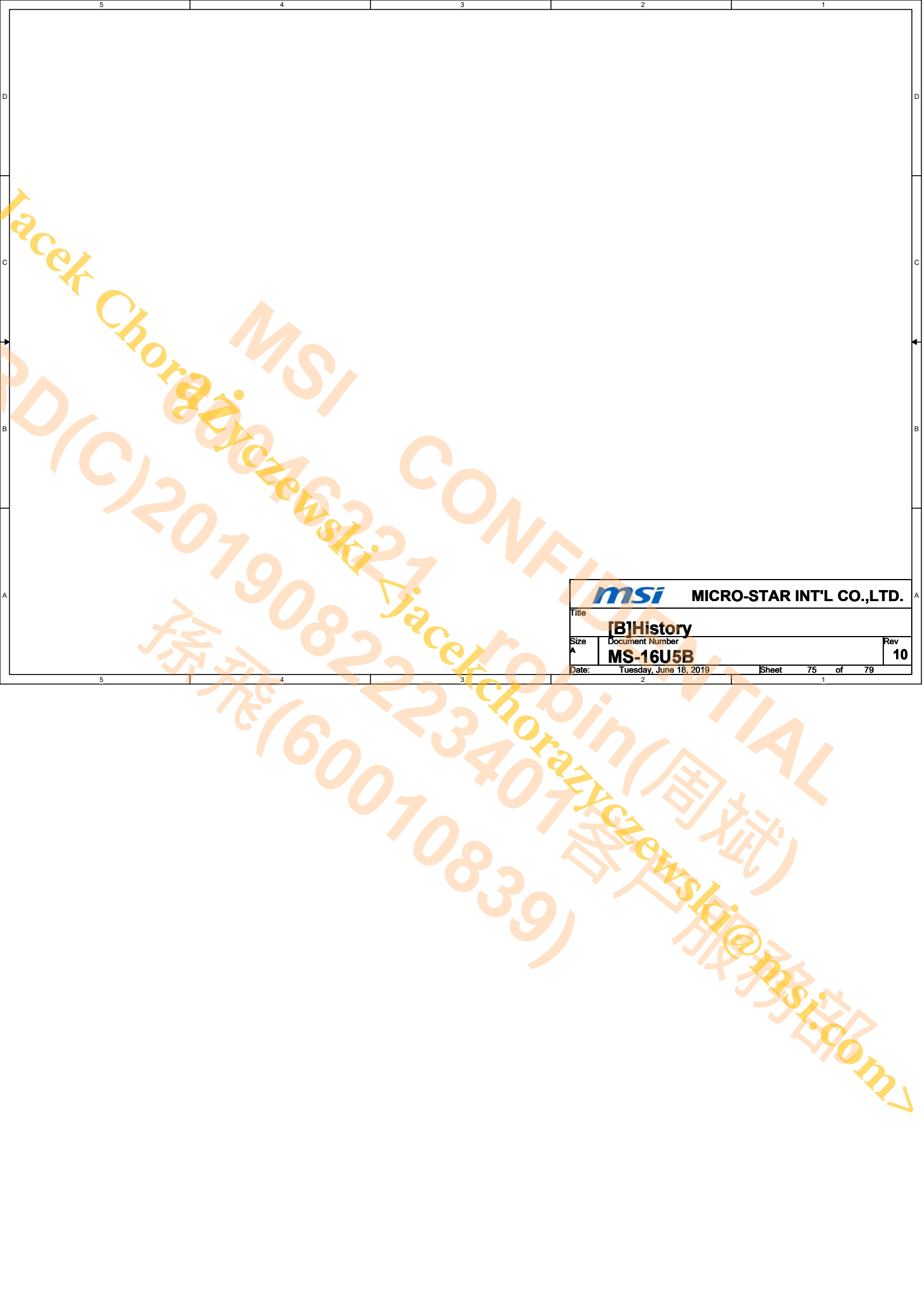



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Size	Document Number
Custom	MS-16U5B
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Tuesday, June 18, 2019	10
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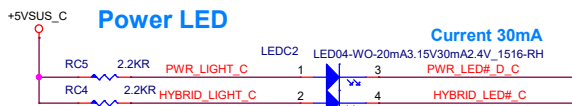
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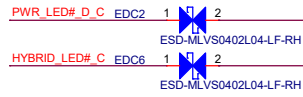
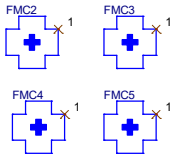
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File MSI USB3.0	
Site Customer	Document Number MS-16U5B
Date Tuesday, June 18, 2019	Sheet 72 of 79



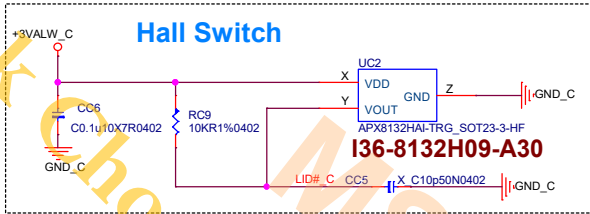
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Date:	Tuesday, June 18, 2019	Sheet	75 of 79



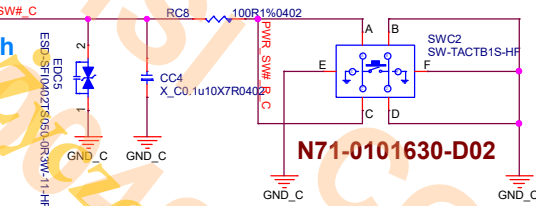
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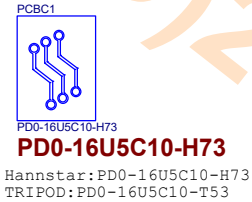
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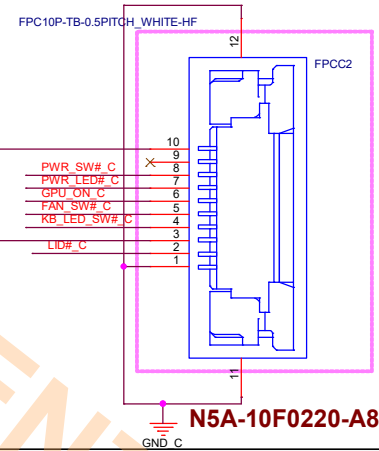
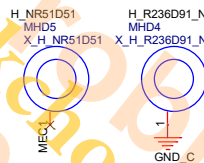
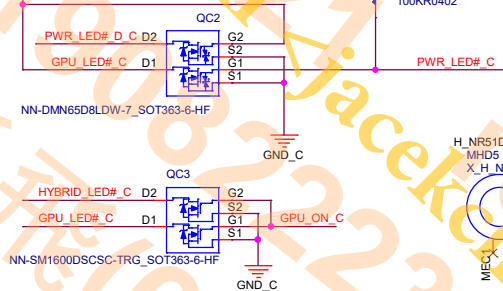
Power Switch



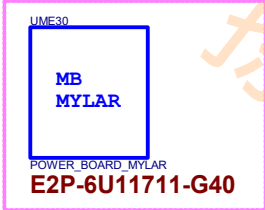
N71-0101630-D02



Control PWR LED



N5A-10F0220-A81




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Title [C]Power Switch			
Size Custom	Document Number MS-16U5C	Rev 10	
Date: Tuesday, June 18, 2019	Sheet 1	of 79	

5 4 3 2 1

2017/02/06

1. Add MHD7, delete MHC13

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		MICRO-STAR INT'L CO.,LTD.	
Title			
[C]History			
Size	Document Number		Rev
A	MS-16U5C		10
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5 4 3 2 1

TOP

Power switch

16U1C

BOT

16U11

10

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Title

TOP

Size

A

Document Number

MS-17E51/MS-16U51

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Date:

Tuesday, June 18, 2019

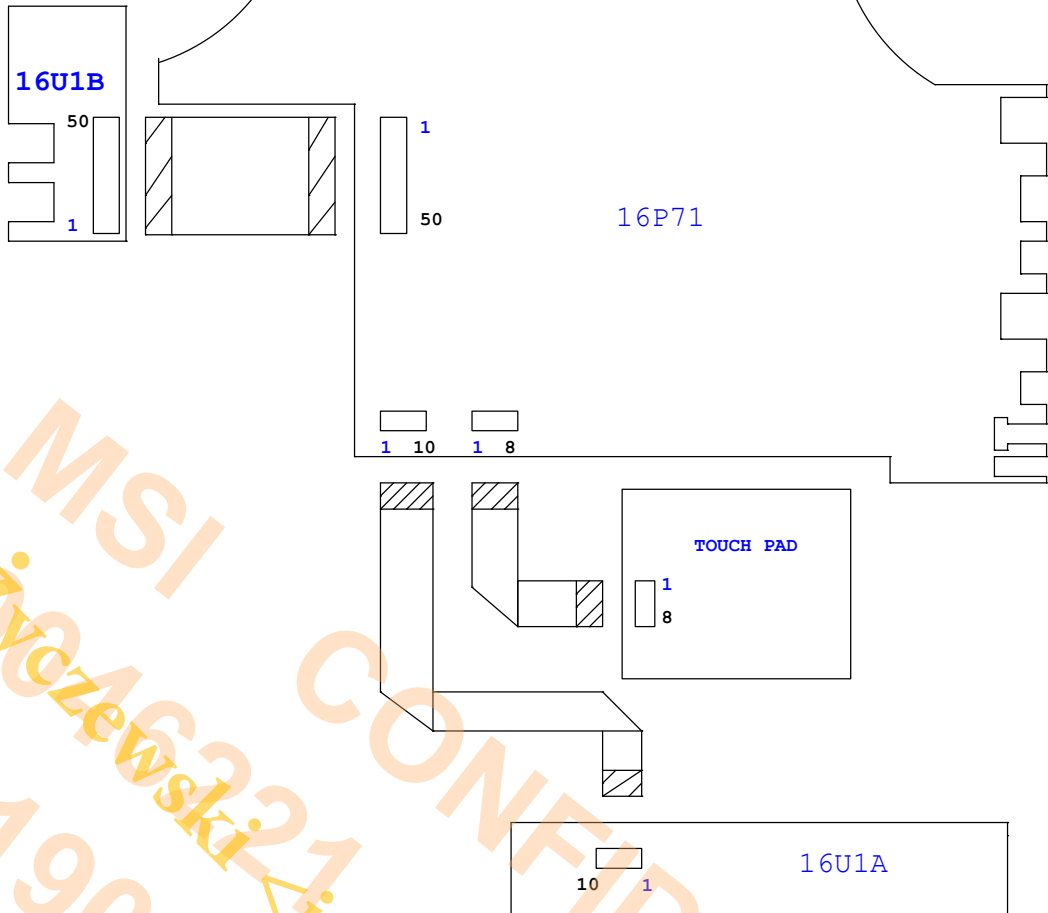
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Bottom VIEW



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Bottom VIEW		
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